COMPACT DISC PLAYER

DP-990SG

SERVICE MANUAL

KENWOOD

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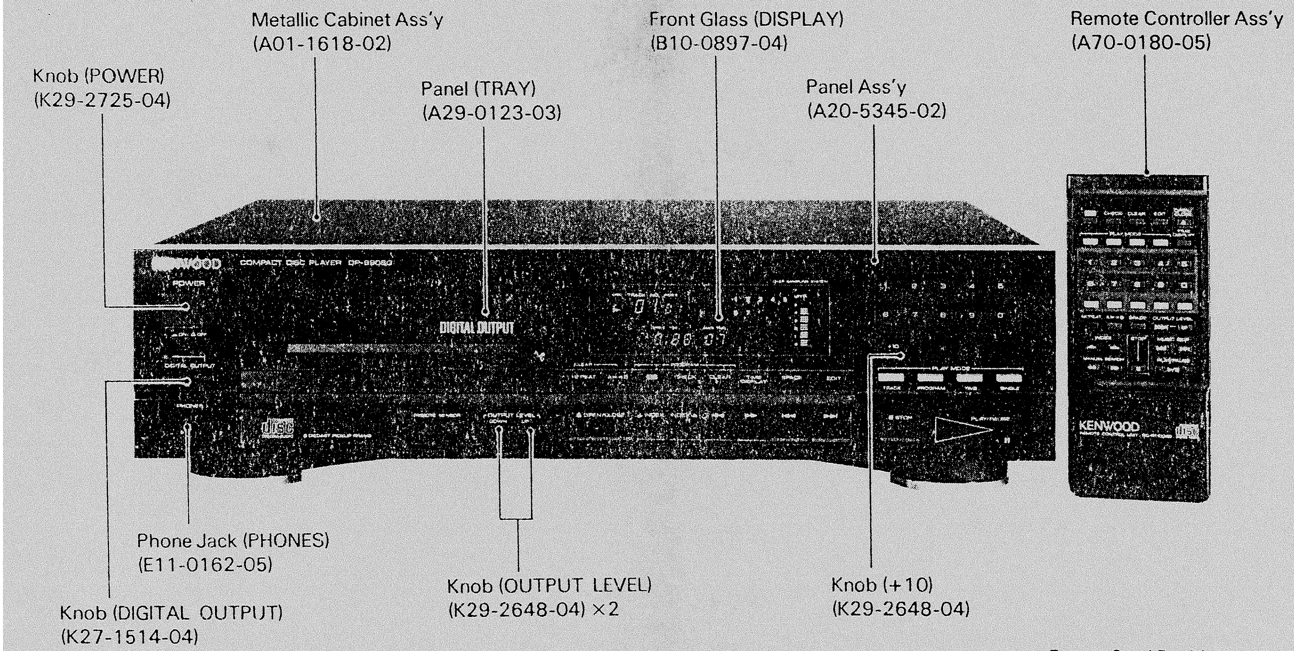
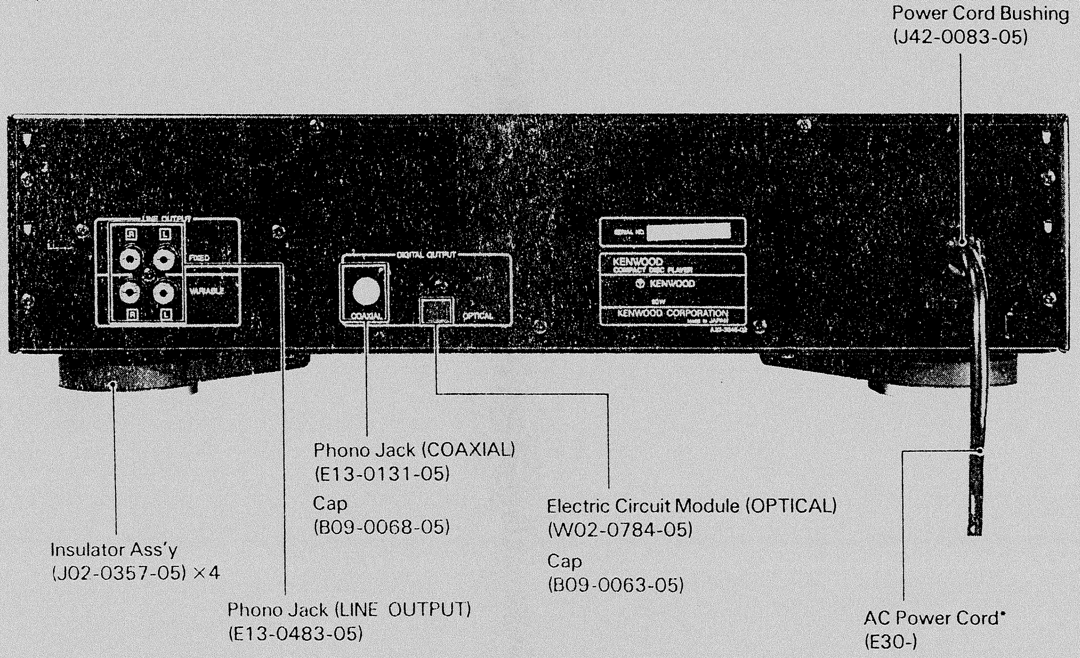
B51-3360-00(B)2846


Metallic Cabinet Ass'y
(A01-1618-02)
Front Glass (DISPLAY)
(B10-0897-04)
Remote Controller Ass'y
(A70-0180-05)
Knob (POWER)
(K29-2725-04)
Panel (TRAY)
(A29-0123-03)
Panel Ass'y
(A20-5345-02)
Phone Jack (PHONES)
(E11-0162-05)
Knob (OUTPUT LEVEL)
(K29-2648-04) ×2
Knob (+10)
(K29-2648-04)
Knob (DIGITAL OUTPUT)
(K27-1514-04)


Power Cord Bushing
(J42-0083-05)
Phono Jack (COAXIAL)
(E13-0131-05)
Cap
(B09-0068-05)
Electric Circuit Module (OPTICAL)
(W02-0784-05)
Cap
(B09-0063-05)
Insulator Ass'y
(J02-0357-05) ×4
Phono Jack (LINE OUTPUT)
(E13-0483-05)
AC Power Cord*
(E30-)

In compliance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

* Refer to parts list on page 85.

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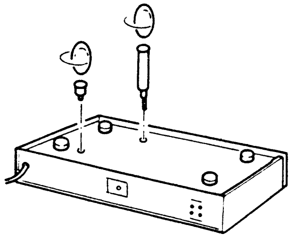
SPECIFICATIONS .... Back cover

TRANSPORTATION SCREW

Transportation screw

Before operation, remove the two red screws attached to the bottom of the unit used during transport from the factory. Remove both screws using a coin, etc. and, after removing, retain them together with the Warranty card and other documents. When the unit is so be transported again, be sure replace the two screws to their original position:

- For the procedure of attaching the transportation screws, refer to page 22.



■ Before transport: tighten the transportation screws

- Before transporting this unit, be sure to tighten the two transportation screws on the bottom of the unit.

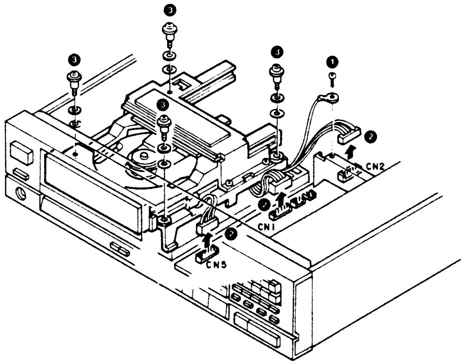
1. Turn ON the power switch when no disc is loaded.
2. Wait a few seconds until the disc OUT indicator comes "ON". Then turn "OFF" the power.

3. Firmly tighten the two transportation screws.

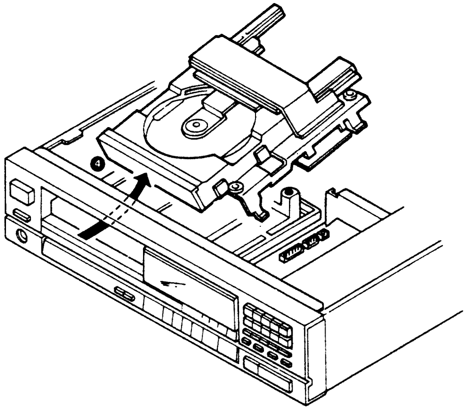
DISASSEMBLY FOR REPAIR

Mechanism assembly removal procedure

1. Remove the screw (❶) retaining the ground lug from the mechanism assembly.
2. Remove the three connectors (❷).
3. Remove the four screws (❸) retaining the mechanism assembly.



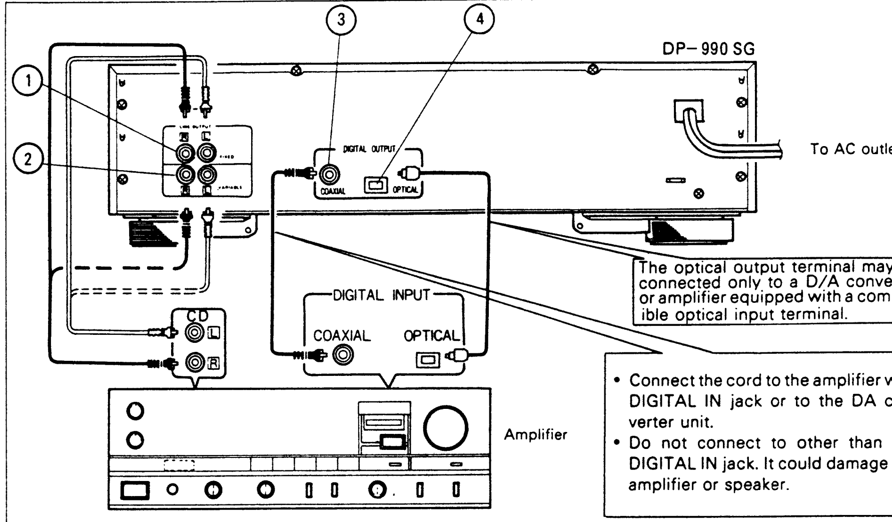
4. Remove the mechanism assembly by pulling out in the direction of the arrow (❹).



SYSTEM CONNECTIONS

Connection precautions

Always turn OFF the power before making connections.
Incorrect connections can cause damage to your audio system. Heed the precautions and follow the dire carefully.



The optical output terminal may connected only to a D/A conve or amplifier equipped with a com ible optical input terminal.

- Connect the cord to the amplifier v DIGITAL IN jack or to the DA c verter unit.
- Do not connect to other than DIGITAL IN jack. It could damage amplifier or speaker.

① **Fixed output (FIXED): Output voltage 2Vrms fixed**
Use these stereo output jacks for connection to a typical amplifier or receiver.

② **Variable output (VARIABLE): Output voltage 0~2Vrms variable**
You can adjust the output level from these jacks to match the signal level of other sources connected to your amplifier or receiver. (May also be used for adjusting recording level by remote control).

③ **Digital output (DIGITAL OUTPUT, COAXIAL) 0.5Vp-p 75 ohms**

④ **Optical output (DIGITAL OUTPUT, OPTIC**
–15dBm~–25dBm

Note:

1. If your amp has both optical and coax digital inputs, only one or the other. Connection to both creates a which can cause undesirable oscillation.
2. Be careful never to kink, twist or bend the optical fiber c excessively.
3. This unit is not necessarily compatible with the optical cables provided by other manufacturers. If connectic not successful, consult your dealer or ser representative.

■ Connection to amplifier or receiver

(The following three methods are possible.)

- **Conventional amplifier connection:**
  Connect the CD player's LINE OUTPUT (FIXED or VARIABLE) to the AUX or CD input jacks on the rear panel of the amp or receiver. Use the supplied cord. Be sure to connect the left (L) and right (R) jacks on the CD player to the corresponding jacks on the amplifier or receiver.
- **Connection to an amplifier equipped with digital input:**
  Use a single coaxial cable to connect the CD player's DIGITAL OUT jack to the digital input jack on the amplifier.
- **Connection to a component equipped with optical fiber cable (OPTICAL INPUT) terminal:**
  Use an optical fiber cable to connect the CD player's (DIGITAL OUT) OPTICAL terminal to the optical input terminal on the other component.

Plug in the AC power cord for the CD playe amplifier.

DP-990SG DP-990SG

CONTROLS AND INDICATORS

❶ **POWER switch**

❷ **DIGITAL OUTPUT indicator**
This illuminates when the digital output switch is on.

❸ **DIGITAL OUTPUT switch**
This switches digital output on and off.

❹ **PHONES jack**
Plug stereo headphones into this jack.

❺ **Dyna-pneumatic suspension**
Designed to safeguard sound quality by isolating the player from adverse external vibrations.

Note:
To maintain the effectiveness of the Dyna-pneumatic suspension, do not place other components or items weighing more than 5kg on top of this unit.

❻ **REMOTE SENSOR window**
This picks up infrared signals from the remote control.

❼ **OUTPUT LEVEL adjustment keys**
These DOWN/UP keys simultaneously adjust both the rear panel VARIABLE output signal level and headphone volume.
The output level setting is shown by the indicators on the right side of the display.

❽ **OPEN/CLOSE key (▲)**
Press once to open the disc tray. Press again to close.

❾ **INDEX keys (⏶ INDEX ⏶)**
Used to specify index numbers within tracks.

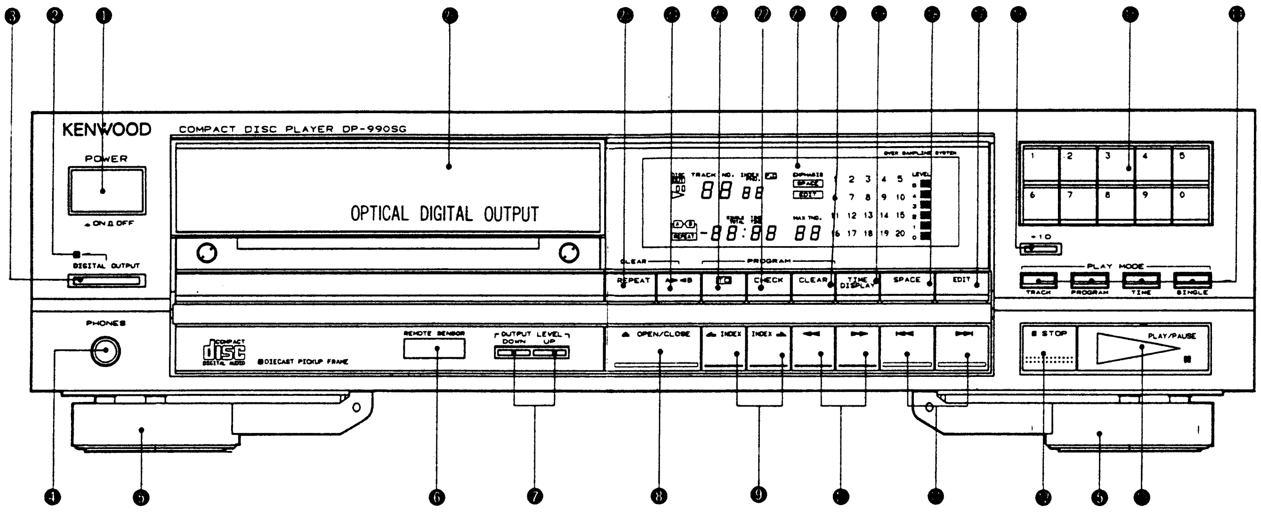
❿ **Manual search keys (◀◀ , ▶▶)**
These keys let you move quickly forward or backward across the disc.

⓫ **Music skip keys (|◀◀ , ▶▶|)**
Used to skip forward to the start of the next track or back to the start of the current or preceding track.

⓬ **STOP key (■)**
Press to stop play.

⓭ **PLAY/PAUSE key (▷/II)**
Press to begin play. Press during play to pause or resume play.

⓮ **PLAY MODE keys**
Used to select the play mode: TRACK, PROGRAM, TIME, or SINGLE.


KENWOOD
COMPACT DISC PLAYER DP-990SG
POWER
▲ON ▲OFF
DIGITAL OUTPUT
OPTICAL DIGITAL OUTPUT
PHONES
COMPACT disc DIGITAL AUDIO
DIECAST PICKUP FRAME
REMOTE SENSOR
OUTPUT LEVEL
DOWN UP
▲ OPEN/CLOSE
INDEX
INDEX
CLEAR
PROGRAM
REPEAT
CHECK
CLEAR
TIME DISPLAY
SPACE
EDIT
+10
PLAY MODE
TRACK
PROGRAM
TIME
SINGLE
■ STOP
PLAY/PAUSE
1
2
3
4
5
6
7
8
9
0

⓯ **Numeric keys (1 ~ 0)**
Used to specify first digit in a number when selecting a tune or setting a time.

⓰ **Plus ten key (+10)**
Adds ten to a number. Used with the numeric keys.

⓱ **EDIT key**
Used to automatically fit tracks into a program of a specified time length.

⓲ **SPACE key**
This causes play to pause for about four seconds between tunes, useful when taping.

⓳ **TIME DISPLAY key**
This switches the time display.

⓴ **CLEAR key**
This erases the last tracks in a program.

㉑ **DISPLAY**

㉒ **CHECK key**
Press to check program contents.

㉓ **TO key**
When programming, this lets you input a number of consecutive tunes starting at a particular track number.

㉔ **A ▶◀ B repeat key**
This key lets you define the beginning (A) and end (B) points of a section of music that you want played repeatedly.

㉕ **REPEAT key**
Used for repeated play.

㉖ **Disc tray**

Display window

① **Disc indicator (DISC)**
Confirms that a disc is in the tray.

② **Disc out indicator (OUT)**
This illuminates (red) when there is no disc in the tray.

③ **Pause indicator (II)**

④ **Play indicator (▶)**

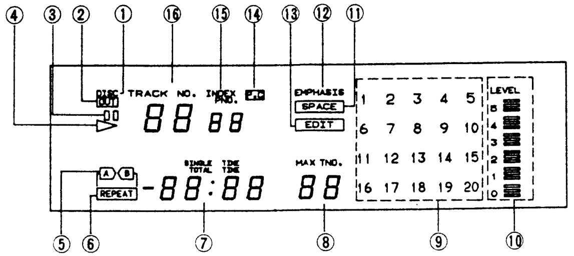
⑤ **A-B repeat indicator (A▷◁B)**

⑥ **REPEAT indicator (REPEAT)**

⑦ **Time counter (TOTAL TIME, SINGLE TIME)**

⑧ **Maximum track number indicator (MAX TNO.)**
Shows the highest track number found on the current disc.

⑨ **Music calendar (1 – 20)**
Indicates the track (selection) numbers on the disc, or shows which selections are programmed for play.


④
③
②
①
⑯
⑮
⑭
⑬
⑫
⑪
DISC
OUT
TRACK NO.
INDEX PNO.
P.C
EMPHASIS
SPACE
EDIT
88 88
1 2 3 4 5
6 7 8 9 10
11 12 13 14 15
16 17 18 19 20
LEVEL
5
4
3
2
1
0
A B
REPEAT
SINGLE TOTAL TIME
-88:88
MAX TNO.
88
⑤
⑥
⑦
⑧
⑨
⑩

⑩ **OUTPUT LEVEL indicator**
Six LEDs show the output level (of the signal from the VARIABLE jacks on the rear panel.) This can be adjusted by remote control or output level adjustment screw on the rearpanel.

⑪ **SPACE indicator (SPACE)**

⑫ **Emphasis indicator (EMPHASIS)**
This confirms that the disc in play was recorded with high frequency emphasis.

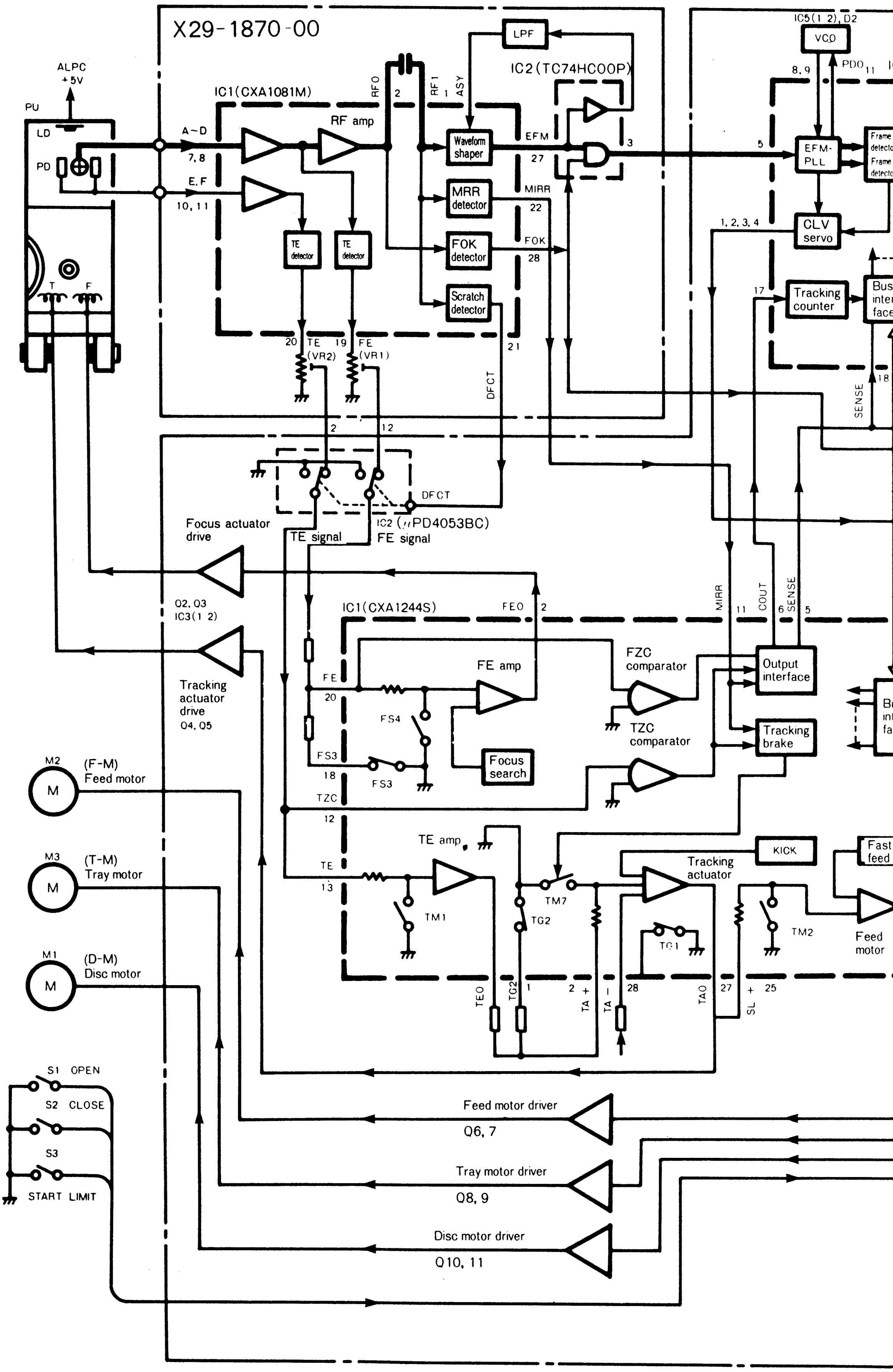
⑬ **Edit indicator (EDIT)**

⑭ **Program check indicator (P.C)**
Lights up when you check program contents.

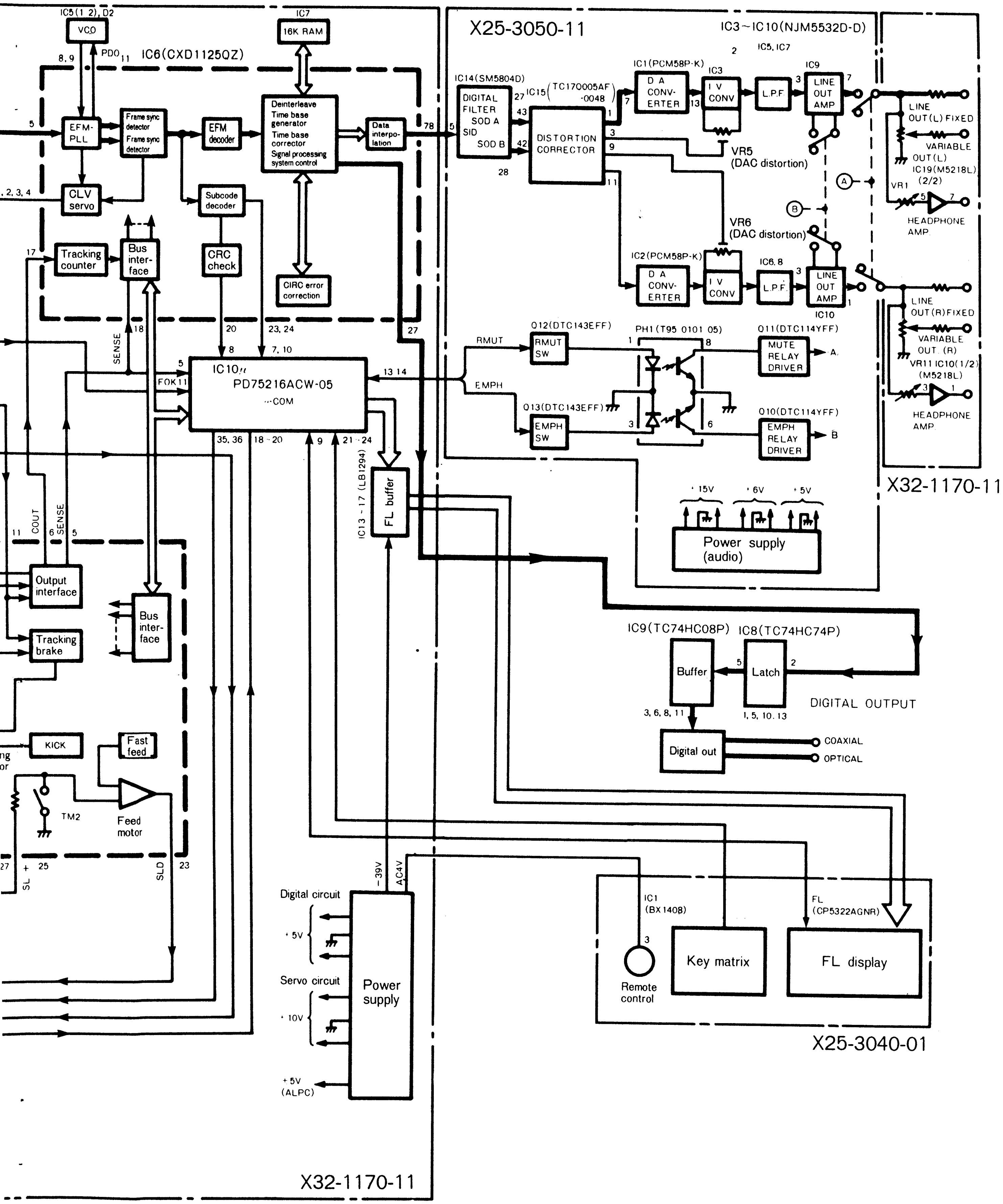
⑮ **Index number (INDEX)/program number (PNO.)**
Shows the current index number within the track. Shows the number of tracks during programming or when checking program contents.

⑯ **Track number display (TRACK NO.)**
Shows the track number (according to the order of the selections on the disc).

BLOCK DIA


X29-1870-00
ALPC
+5V
PU
LD
PD
T
F
A~D
7, 8
E, F
10, 11
IC1(CXA1081M)
RF amp
RFO
2
RF1
1
ASY
LPF
IC2(TC74HC00P)
Waveform shaper
EFM
27
MRR detector
MIRR
22
FOK detector
FOK
28
Scratch detector
21
DFCT
TE detector
TE detector
20
TE
(VR2)
19
FE
(VR1)
3
IC5(1/2), D2
VCO
8, 9
PDO
11
5
EFM-PLL
Frame detector
Frame detector
1, 2, 3, 4
CLV servo
17
Tracking counter
Bus interface
18
SENSE
2
12
DFCT
IC2 (μPD4053BC)
TE signal
FE signal
Focus actuator drive
Q2, Q3
IC3(1/2)
Tracking actuator drive
Q4, Q5
IC1(CXA1244S)
FEO
2
MIRR
11
COUT
6
SENSE
5
FE
20
FE amp
FS4
FS3
18
FS3
Focus search
FZC comparator
TZC comparator
Output interface
Tracking brake
TZC
12
TE
13
TE amp
TM1
TM7
TG2
KICK
Tracking actuator
TG1
TM2
Fast feed
Feed motor
TEO
TG2
1
2
TA +
TA −
28
TAO
27
SL
+
25
M2
(F-M)
Feed motor
M3
(T-M)
Tray motor
M1
(D-M)
Disc motor
M
S1 OPEN
S2 CLOSE
S3
START LIMIT
Feed motor driver
Q6, 7
Tray motor driver
Q8, 9
Disc motor driver
Q10, 11

BLOCK DIAGRAM


IC5(1/2), D2
VCO
IC7
16K RAM
8, 9
PDO 11
IC6(CXD1125QZ)
5
EFM-PLL
Frame sync detector
Frame sync detector
EFM decoder
Deinterleave
Time base generator
Time base corrector
Signal processing system control
Data interpolation
78
CLV servo
Subcode decoder
17
Tracking counter
Bus inter-face
CRC check
CIRC error correction
SENSE
18
20
23, 24
27
8
7, 10
5
FOK 11
IC10 μPD75216ACW-05
μCOM
13 14
35, 36
18 - 20
9
21 - 24
IC13 - 17 (LB1294)
FL buffer
COUT
SENSE
11
6
5
Output interface
Bus inter-face
Tracking brake
KICK
Fast feed
TM2
Feed motor
27
25
SL
SLD
23
−39V
AC4V
Digital circuit
+5V
Servo circuit
+10V
+5V (ALPC)
Power supply
X32-1170-11
X25-3050-11
IC3 ~ IC10(NJM5532D-D)
2
IC5, IC7
IC1(PCM58P-K)
IC3
IC9
IC14(SM5804D)
IC15(TC170005AF -0048)
DIGITAL FILTER
SOD A
SID
SOD B
27
43
42
28
5
DISTORTION CORRECTOR
1
3
9
11
7
D A CONV-ERTER
13
I V CONV
L.P.F.
3
LINE OUT AMP
7
VR5 (DAC distortion)
VR6 (DAC distortion)
A
B
IC2(PCM58P-K)
D A CONV-ERTER
I V CONV
IC6, 8
L.P.F.
3
LINE OUT AMP
1
IC10
LINE OUT(L) FIXED
VARIABLE OUT(L)
IC19(M5218L) (2/2)
VR1
5
7
HEADPHONE AMP
LINE OUT(R) FIXED
VARIABLE OUT (R)
VR11 IC10(1/2) (M5218L)
3
1
HEADPHONE AMP
X32-1170-11
Q12(DTC143EFF)
RMUT
RMUT SW
PH1(T95 0101 05)
1
8
Q11(DTC114YFF)
MUTE RELAY DRIVER
A
EMPH
Q13(DTC143EFF)
EMPH SW
3
6
Q10(DTC114YFF)
EMPH RELAY DRIVER
B
+15V
+6V
+5V
Power supply (audio)
IC9(TC74HC08P)
IC8(TC74HC74P)
Buffer
5
Latch
2
3, 6, 8, 11
1, 5, 10, 13
DIGITAL OUTPUT
Digital out
COAXIAL
OPTICAL
IC1 (BX1408)
3
Remote control
Key matrix
FL (CP5322AGNR)
FL display
X25-3040-01

CIRCUIT DESCRIPTION

Description of components

Display Unit (X25-3040-01)

Component		Use/Function	Operation/Condition/Compatibility
IC1	BX1408	Remote control signal receiving device	Converts the infrared signal from the remote control into logic signal
IC2	TC74HC174F	D-type flip-flop	Controls lamps and LEDs for each mode
IC3	TD62003AP	Transistor array	Transistor array drives lamps and LEDs for each mode

D/A Converter Unit (X25-3050-XX)

Component		Use/Function	Operation/Condition/Compatibility
IC1,2	PCM56P-K	D/A converter	Resistance ladder type D/A converter; converts digital data into the volume of analog data.
IC3,4	NJM5532D-D	I-V converter	(1/2) Converts current output of D/A converter into voltage. (2/2) Generates offset voltage for distortion compensation.
IC5～8	NJM5532D-D	Op amp	Consists GIC (general impedance converter) in LPF
IC9,10	NJM5532D-D	Op amp	Buffer amp and output amp
IC13	M5220P	Op amp	Error amp for ±15 V constant power supply
IC14	SM5804D	Digital filter	4 times oversampling digital filter
IC15	TC17Q005AF-0048	D/A distortion compensator	D/A distortion compensation, 2SB detection circuit
IC16	M5F79M06L	3-pin regulator	−6 V (−VCC) power supply for D/A converter circuit
IC17	M5F78M06L	3-pin regulator	+6 V (+VCC) power supply for D/A converter circuit
IC22	M5F79M05L	3-pin regulator	−5 V (−VL) power supply for D/A converter circuit
IC23	M5F78M05L	3-pin regulator	+5 V (+VL) power supply for D/A converter circuit
IC24	M51951ASL	Reset IC	Reset IC for digital filter
Q2	2SD1266(P)	Ripple filter	Ripple filter for +15 V constant power supply
Q3	2SB941(P)	Ripple filter	Ripple filter for −15 V constant power supply
Q10	DTC114YFF	Switch	Relay driver for deemphasis
Q11	DTC114YFF	Switch	Relay driver for muting
Q12	DTC143EFF	Switch	Muting photocoupler driver
Q13	DTC143EFF	Switch	Photocoupler driver for deemphasis
Q14	2SA733(A) (Q,F)	Transistor	For power supply of photocoupler output
D17	E-102	Constant current diode	Constant current diode for ±15 V constant power supply

Control Circuit Unit (X29-1870-00)

Component		Use/Function	Operation/Condition/Compatibility
IC1	CXA1081M	RF amp	Focus error signal generation, tracking error signal generation, RF signal generation ar phase compensation, and auto symmetry compensation circuit
IC2	TC74HC00P	NAND gate	EFMT signal waveform detection, auto symmetry signal detection
Q1	2SC2878	Switch	Focus error amp bias select switch

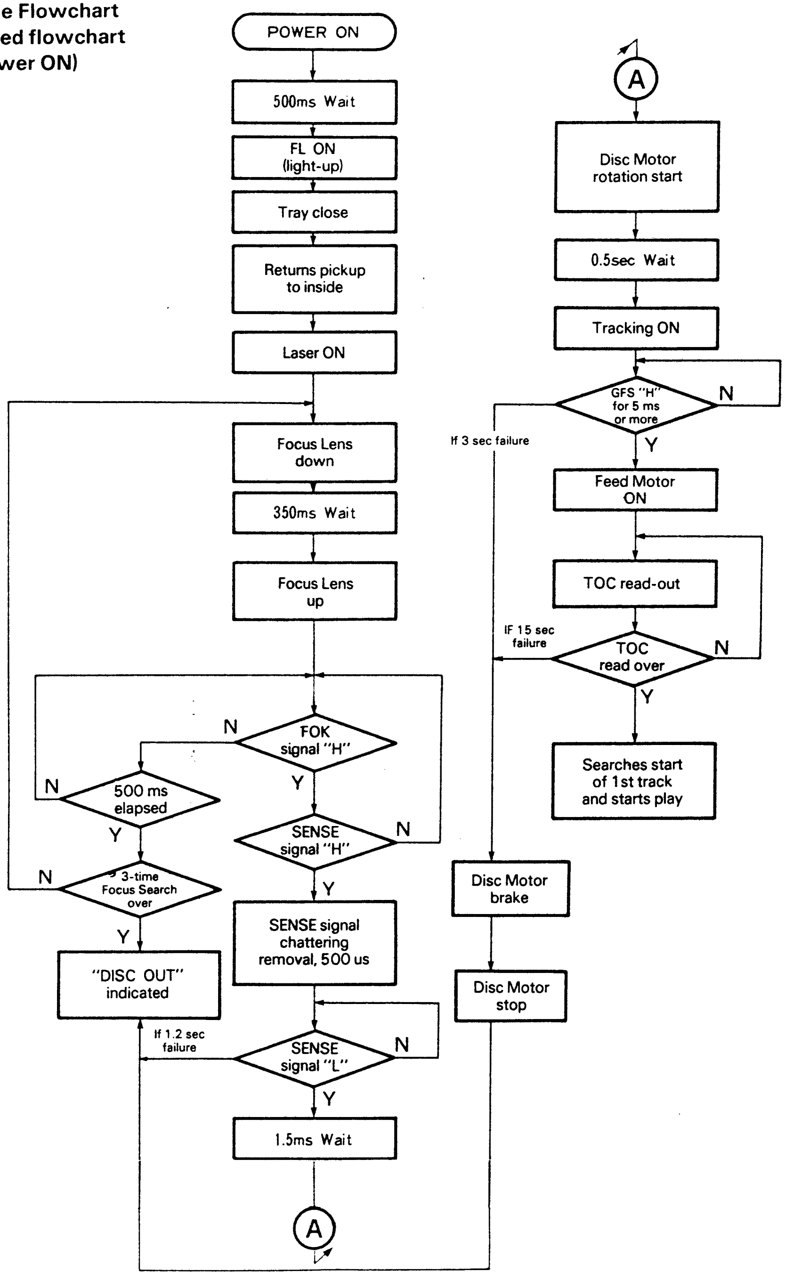
CIRCUIT DESCRIPTION

CD Player Unit (X32-1170-11)

Component		Use/Function	Operation/Condition/Compatibility
IC1	CXA1244S	Servo IC	Various pulse generation for focus servo, tracking servo, and feed servo (CX20108 shrink type)
IC2	μPD4053BC	Analog switch	Receives scratch detection signal (DFCT signal from pin 21 of CXA1081M) and turns focus and tracking servo OFF when scratches are present.
IC3	M5218P-K	Op amp	(1/2) For focus servo phase compensation (2/2) For tracking servo phase compensation
IC4	NJM4558D	Op amp	(1/2) For VARIABLE volume motor drive (2/2) For tray motor drive
IC5	M5218P-K	Op amp	(1/2) PLL compensation circuit (LPF+amp) (2/2) CLV compensation circuit (LPF+level shifter)
IC6	CXD1125QZ	Digital signal processing LSI	Executes all digital signal processing including EFM data decoding, error correction, interpolation, PLL circuit, CLV servo and digital out, etc.
IC7	CXK5816SP	Static RAM	Signal processing RAM (16K)
IC9	TC74HC08P	AND gate	Buffer amp for digital out, and reset signal generator when power is ON/OFF
IC10	μPD75216 ACW-051	Microprocessor	Display, each key input processing and servo IC control.
IC11	M51951ASL	Reset IC	Generates reset signal when power is ON/OFF
IC12	LB1344N	Linear scale level meter IC	Outputs VARIABLE volume position indication
IC13～17	LB1294	FL driver IC	IC for driving FL display
IC18	M5F78M05L	3-pin regulator	+5 V power supply for digital and servo circuits
IC19	M5218L	Op amp	Headphone amp
IC20	NJM4558D	Op amp	(1/2) Rising and trailing control for +5 V and −5 V power supply (2/2) Supplies +5 V for ALPC, and controls laser ON/OFF
Q1	2SC2878	Switch	Focus gain select
Q2	2SC3940A	Driver	Focus actuator driver
Q3	2SA1534A	Driver	Focus actuator driver
Q4	2SC3940A	Driver	Tracking actuator driver
Q5	2SA1534A	Driver	Tracking actuator driver
Q6	2SC3940A	Driver	Feed motor driver
Q7	2SA1534A	Driver	Feed motor driver
Q8	2SC3940A	Driver	Tray motor driver
Q9	2SA1534A	Driver	Tray motor driver
Q10	2SC3940A	Driver	Disc motor driver
Q11	2SA1534A	Driver	Disc motor driver
Q12	2SD1266	Driver	VARIABLE volume motor driver
Q13	2SB772	Driver	VARIABLE volume motor driver
Q14	2SC1685	Ripple filter	Power supply for FL driver (+6.6 V)
Q15	2SC945(A) (Q,P)	Switch	FL driver switch
Q16	2SA733(A) (Q,P)	Level shifter	Level shifter for FL driver
Q17	2SC3940A	Ripple filter	Power supply for lamps and LEDs for each mode (+7.5 V)
Q18	2SA954	Ripple filter	Power supply for FL reference voltage (−32 V)
Q19	2SA1127NC	Ripple filter	−5 V power supply
Q20	2SC3940A	Ripple filter	+5 V power supply (for ALPC)
Q21,22	2SC3940A	Driver	Headphone amp driver
Q23,24	2SA1534A	Driver	Headphone amp driver
Q25	DTA124EN	Digital transistor switch	Controls focus offset voltage by the MUTE signal
Q26	DTA124EN	Digital transistor switch	Selects focus gain by the FGSW signal

CIRCUIT DESCRIPTION

Set Mode Flowchart (Simplified flowchart after power ON)

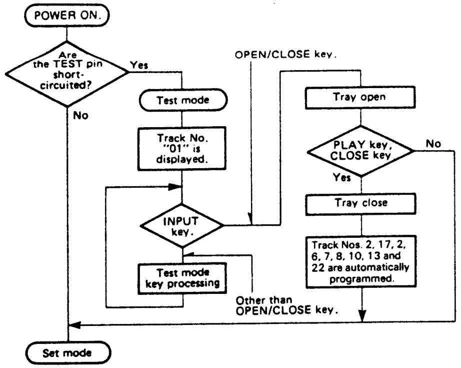

POWER ON
500ms Wait
FL ON (light-up)
Tray close
Returns pickup to inside
Laser ON
Focus Lens down
350ms Wait
Focus Lens up
FOK signal "H"
N
Y
500 ms elapsed
N
Y
3-time Focus Search over
N
Y
"DISC OUT" indicated
SENSE signal "H"
N
Y
SENSE signal chattering removal, 500 us
SENSE signal "L"
N
Y
If 1.2 sec failure
1.5ms Wait
A
A
Disc Motor rotation start
0.5sec Wait
Tracking ON
GFS "H" for 5 ms or more
N
Y
If 3 sec failure
Feed Motor ON
TOC read-out
TOC read over
N
Y
IF 15 sec failure
Searches start of 1st track and starts play
Disc Motor brake
Disc Motor stop

Test mode

If the TEST pins are short-circuited when the power is turned ON, the microprocessor enters test mode. With the microprocessor set to test mode, each operation can be easily checked after making a repaire or adjustment.

With the DP-990SG, the microprocessor can be set to test mode by short-circuiting pin 6 and pin 7 of the CD PLAYER UNIT (X32-1170-11).

Note': "Set mode" shows the normal status.

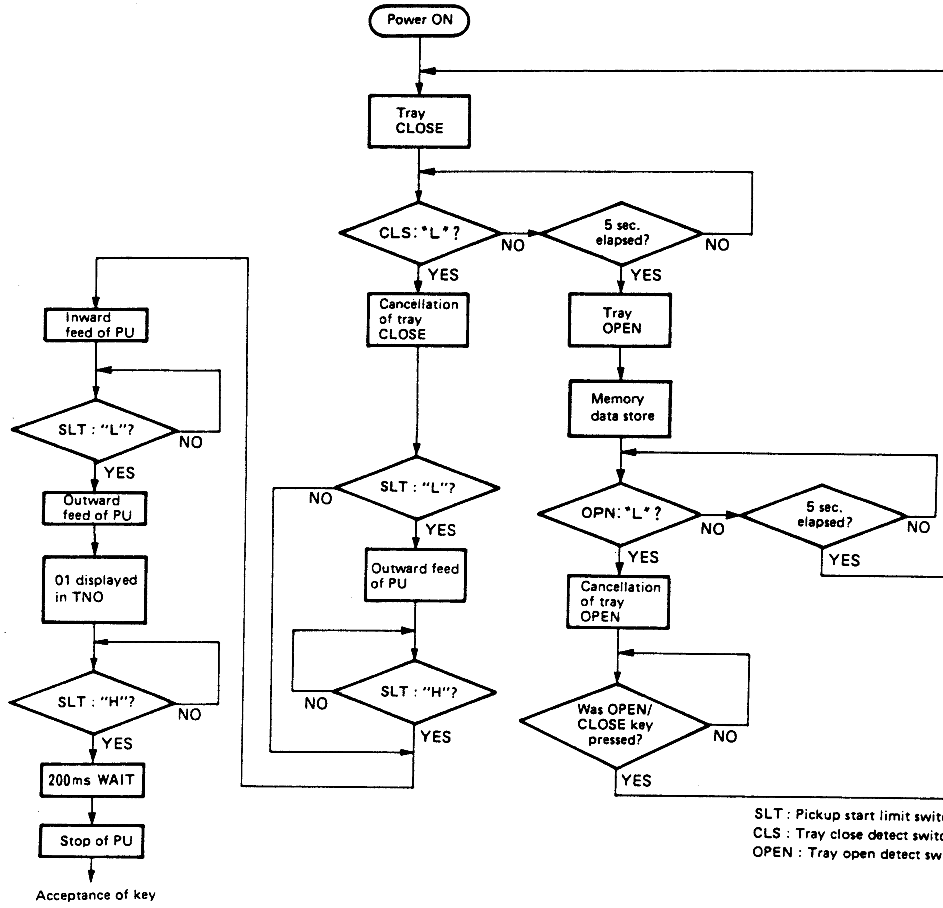

POWER ON.
Are the TEST pin short-circuited?
Yes
No
Test mode
Track No. "01" is displayed.
INPUT key.
Test mode key processing
OPEN/CLOSE key.
Tray open
PLAY key, CLOSE key
No
Yes
Tray close
Track Nos. 2, 17, 2, 6, 7, 8, 10, 13 and 22 are automatically programmed.
Other than OPEN/CLOSE key.
Set mode

- **Effective keys in the Test mode and their functions**

<table>
<tr><th>No.</th><th>Input key</th><th>Function</th><th>Track No. display</th></tr>
<tr><td>1</td><td>PLAY</td><td>(1) Focus servo .... ON.
(2) Tracking servo .... ON.
(3) Feed servo .... ON.
When the key is pressed in the Stop mode, the servoes are switched ON automatically in the order from (1) to (3).</td><td>TRACK NO.
05
↓
Displayed for a few seconds after (1) to (3).
↓
Disc's Track No. is displayed.</td></tr>
<tr><td>2</td><td>CHECK</td><td>(1) Focus servo .... ON.
(2) Tracking servo .... OFF.
(3) Feed servo .... OFF.</td><td>TRACK NO.
03</td></tr>
<tr><td>3</td><td>CLEAR</td><td>(1) Focus servo .... ON.
(2) Tracking servo .... ON.
(3) Feed servo .... OFF.</td><td>TRACK NO.
04</td></tr>
<tr><td>4</td><td>STOP</td><td>(1) Focus servo .... OFF.
(2) Tracking servo .... OFF.
(3) Feed servo .... OFF.</td><td>TRACK NO.
01</td></tr>
<tr><td>5</td><td>REPEAT</td><td>(1) Tray open
(2) Laser................................ON.
When the tray is closed by pressing it, +10 function will be released.
The TRACK NO. display shows "01".</td><td>TRACK NO
02</td></tr>
<tr><td>6</td><td>▶▶</td><td>In Stop mode : Moves the PU slightly to the outer tracks.
With feed servo ON : Switches the tracking gain to "H".</td><td></td></tr>
<tr><td>7</td><td>◀◀</td><td>In Stop mode : Moves the PU slightly to the inner tracks.
With feed servo ON : Switches the tracking gain to "L".</td><td></td></tr>
<tr><td>8</td><td>Numeric (digit) keys (0~9)</td><td>Jumps the number of tracks as follows:
<table>
<tr><td>Key</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr>
<tr><td>Number of tracks</td><td>1</td><td>4</td><td>16</td><td>32</td><td>1000</td></tr>
<tr><td>Direction</td><td colspan="5">Outward</td></tr>
<tr><td>Key</td><td>6</td><td>7</td><td>8</td><td>9</td><td>0</td></tr>
<tr><td>Number of tracks</td><td>1</td><td>4</td><td>16</td><td>32</td><td>1000</td></tr>
<tr><td>Direction</td><td colspan="5">Inward</td></tr>
</table></td><td></td></tr>
<tr><td>9</td><td>OPEN/CLOSE</td><td>When the tray is opened and the closed again in test mode, TRACK NOs 2, 17, 2, 6, 7, 8, 10, 13 and 22 are automatically programmed.
Opening the tray again will cause the unit to enter set mode.</td><td></td></tr>
</table>

Flow chart of test mode

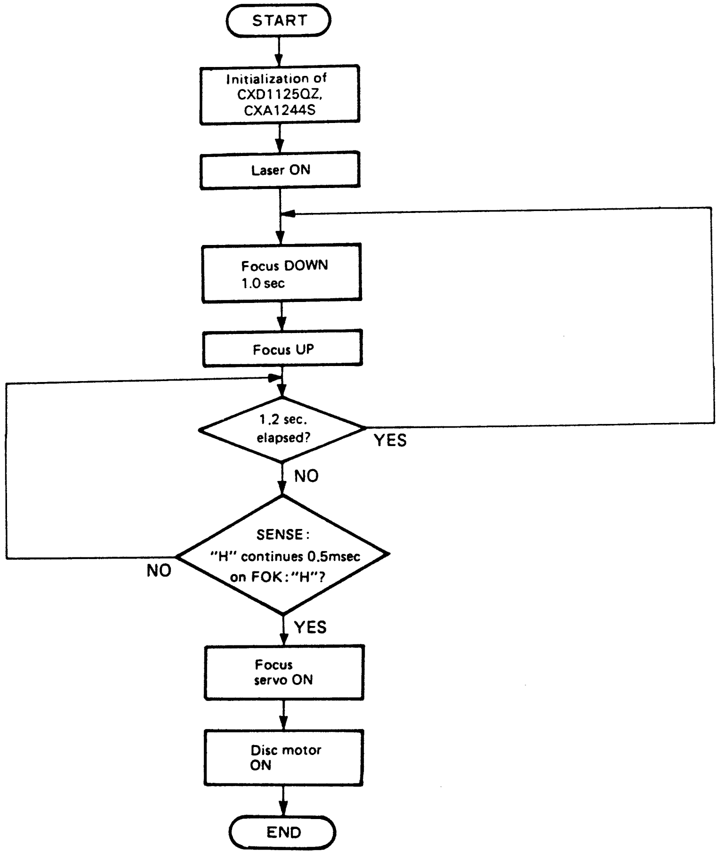
- **Flow chart from tray OPEN status after power ON**


Power ON
Tray CLOSE
CLS: "L"?
NO
YES
5 sec. elapsed?
NO
YES
Cancellation of tray CLOSE
Tray OPEN
Memory data store
OPN: "L"?
NO
YES
5 sec. elapsed?
NO
YES
Cancellation of tray OPEN
Was OPEN/CLOSE key pressed?
NO
YES
SLT : "L"?
NO
YES
Outward feed of PU
SLT : "H"?
NO
YES
Inward feed of PU
SLT : "L"?
NO
YES
Outward feed of PU
01 displayed in TNO
SLT : "H"?
NO
YES
200ms WAIT
Stop of PU
Acceptance of key

SLT : Pickup start limit swit
CLS : Tray close detect swit
OPEN : Tray open detect sw

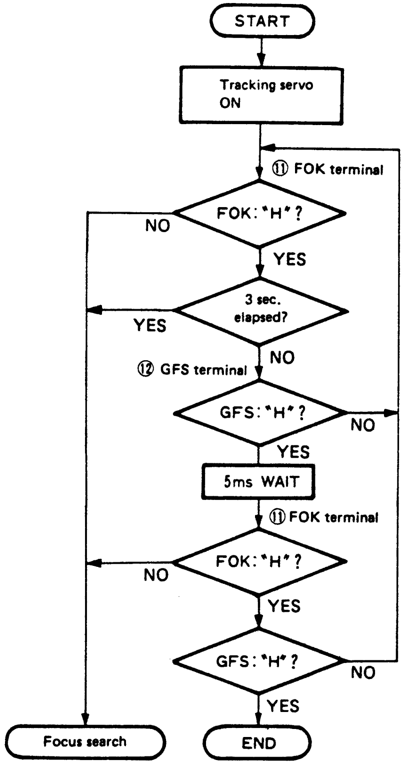
CIRCUIT DESCRIPTION

- **Focus search & focus servo ON**

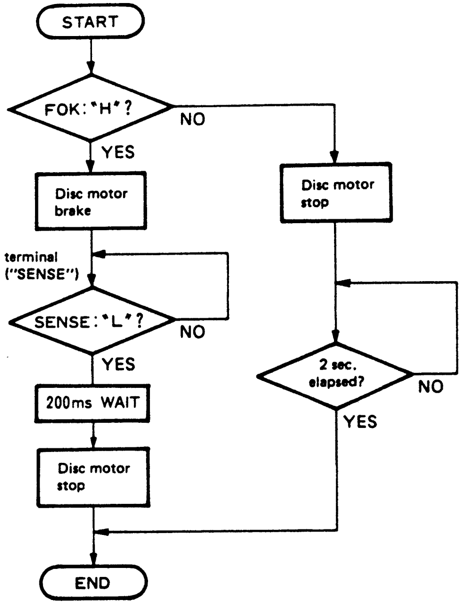

START
Initialization of CXD1125QZ, CXA1244S
Laser ON
Focus DOWN 1.0 sec
Focus UP
1.2 sec. elapsed?
YES
NO
SENSE: "H" continues 0.5msec on FOK: "H"?
NO
YES
Focus servo ON
Disc motor ON
END

CIRCUIT DESCRIPTION

- **Tracking servo ON**

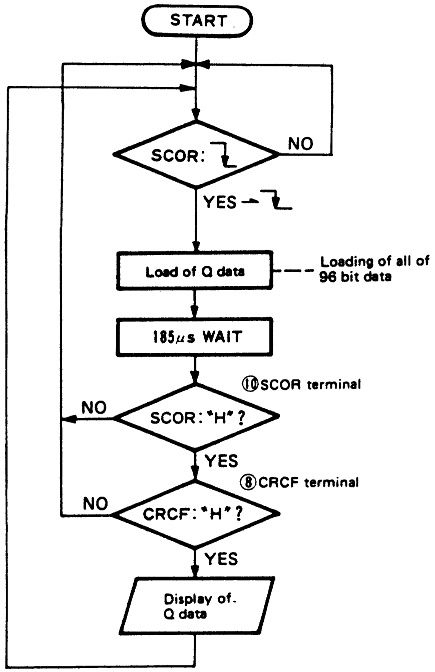

START
Tracking servo ON
⑪ FOK terminal
FOK: "H"?
NO
YES
3 sec. elapsed?
YES
NO
⑫ GFS terminal
GFS: "H"?
NO
YES
5ms WAIT
⑪ FOK terminal
FOK: "H"?
NO
YES
GFS: "H"?
NO
YES
Focus search
END

- **Disc motor stop**

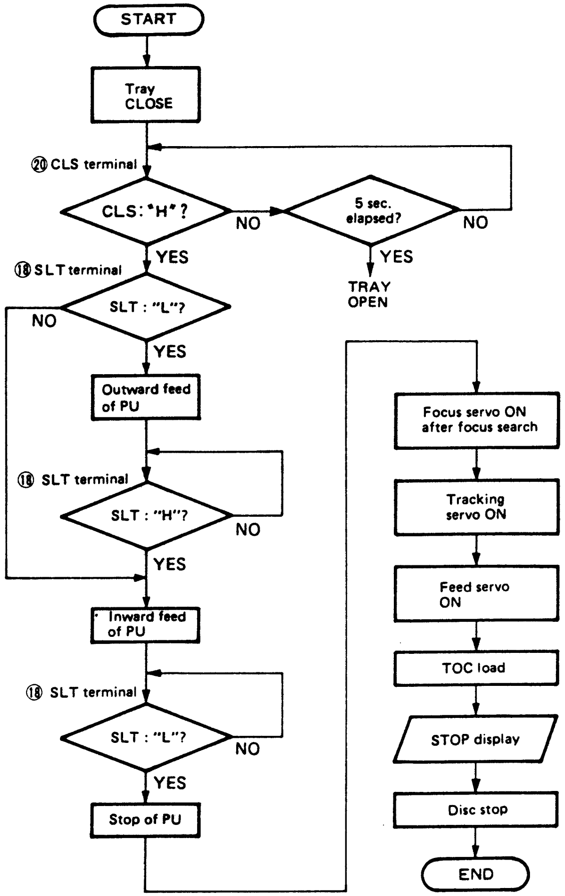

START
FOK: "H"?
NO
YES
Disc motor brake
⑤ terminal ("SENSE")
SENSE: "L"?
NO
YES
200ms WAIT
Disc motor stop
Disc motor stop
2 sec. elapsed?
NO
YES
END

CIRCUIT DESCRIPTION

- **From loading of Q data to display**


START
SCOR: ⅂
NO
YES → ⅂
Load of Q data
Loading of all of 96 bit data
185μs WAIT
⑩SCOR terminal
NO
SCOR: "H"?
YES
⑧CRCF terminal
NO
CRCF: "H"?
YES
Display of. Q data

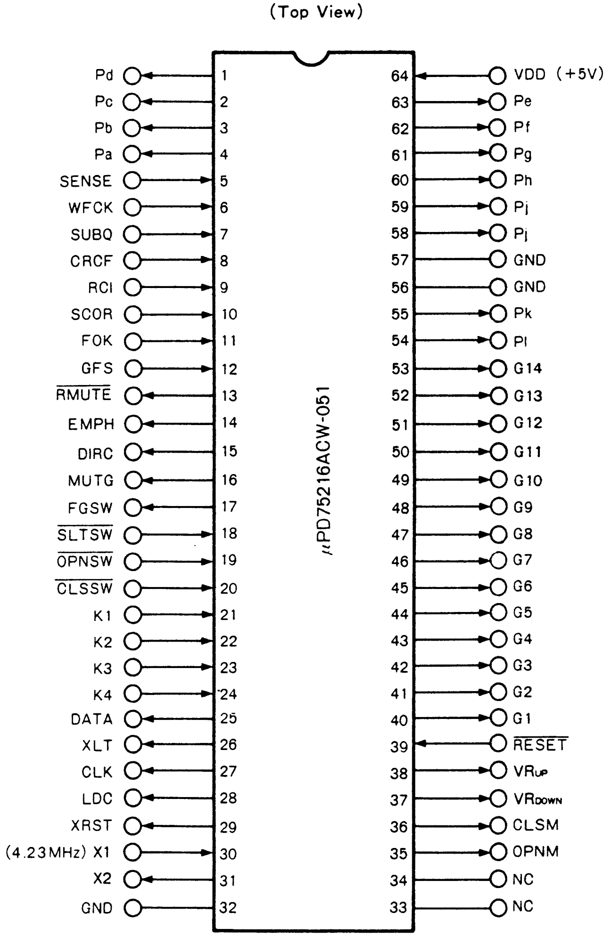
- **Flow chart from the time the tray opens until the STOP indicator lights, after pressing the tray.**


START
Tray CLOSE
⑳CLS terminal
CLS: "H"?
NO
5 sec. elapsed?
NO
YES
TRAY OPEN
YES
⑱SLT terminal
SLT: "L"?
NO
YES
Outward feed of PU
⑱ SLT terminal
SLT: "H"?
NO
YES
Inward feed of PU
⑱ SLT terminal
SLT: "L"?
NO
YES
Stop of PU
Focus servo ON after focus search
Tracking servo ON
Feed servo ON
TOC load
STOP display
Disc stop
END

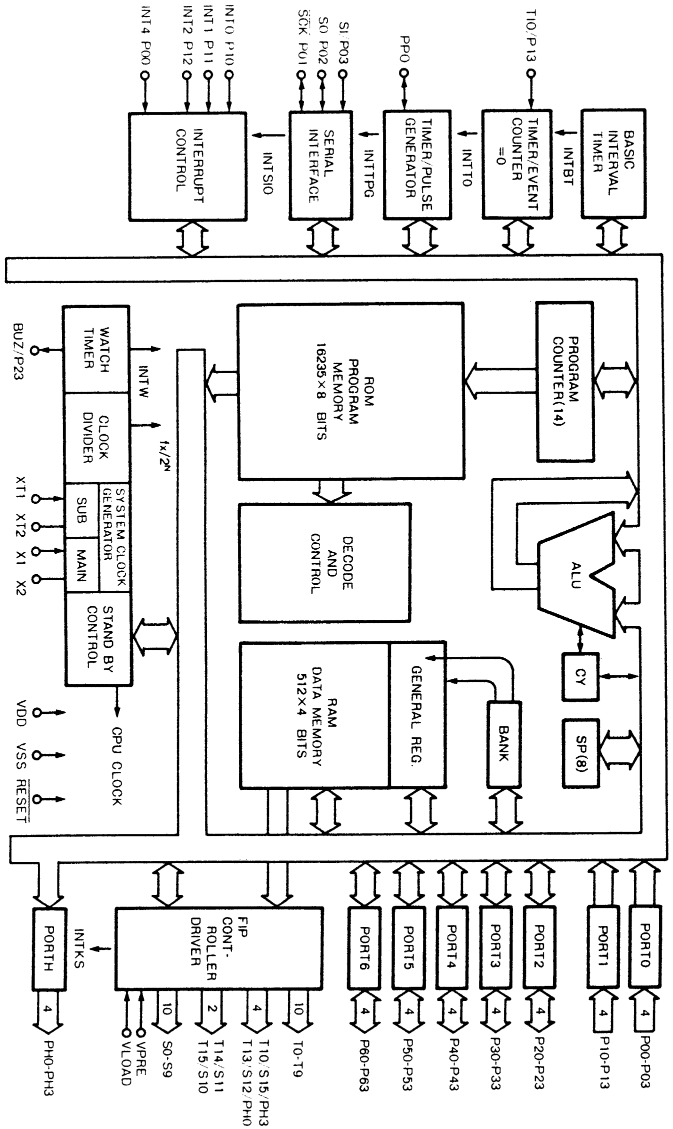
CIRCUIT DESCRIPTION

Microprocessor μPD75216ACW-051 (X32-1170-11: IC10)

Terminal connection diagram


(Top View)
μPD75216ACW-051
Pd 1
Pc 2
Pb 3
Pa 4
SENSE 5
WFCK 6
SUBQ 7
CRCF 8
RCI 9
SCOR 10
FOK 11
GFS 12
RMUTE 13
EMPH 14
DIRC 15
MUTG 16
FGSW 17
SLTSW 18
OPNSW 19
CLSSW 20
K1 21
K2 22
K3 23
K4 24
DATA 25
XLT 26
CLK 27
LDC 28
XRST 29
(4.23MHz) X1 30
X2 31
GND 32
64 VDD (+5V)
63 Pe
62 Pf
61 Pg
60 Ph
59 Pi
58 Pj
57 GND
56 GND
55 Pk
54 Pl
53 G14
52 G13
51 G12
50 G11
49 G10
48 G9
47 G8
46 G7
45 G6
44 G5
43 G4
42 G3
41 G2
40 G1
39 RESET
38 VRUP
37 VRDOWN
36 CLSM
35 OPNM
34 NC
33 NC

CIRCUIT DESCRIPTION


INTERRUPT CONTROL
SERIAL INTERFACE
TIMER/PULSE GENERATOR
TIMER/EVENT COUNTER =0
BASIC INTERVAL TIMER
INT4 P00
INT2 P12
INT1 P11
INT0 P10
$\overline{SCK}$ P01
SO P02
SI P03
PPO
TI0/P13
INTSIO
INTPG
INTTO
INTBT
WATCH TIMER
CLOCK DIVIDER
SYSTEM CLOCK GENERATOR
SUB
MAIN
STAND BY CONTROL
BUZ/P23
INTW
fx/2N
X1
X2
XT1
XT2
CPU CLOCK
VDD
VSS
$\overline{RESET}$
ROM PROGRAM MEMORY 16235×8 BITS
PROGRAM COUNTER(14)
DECODE AND CONTROL
ALU
CY
SP(8)
RAM DATA MEMORY 512×4 BITS
GENERAL REG.
BANK
PORTH
FIP CONTROLLER DRIVER
INTKS
PORT6
PORT5
PORT4
PORT3
PORT2
PORT1
PORT0
PH0-PH3
VLOAD
VPRE
S0-S9
T14/S11
T15/S10
T10/S15/PH3
T13/S12/PH0
T0-T9
P60-P63
P50-P53
P40-P43
P30-P33
P20-P23
P10-P13
P00-P03
4
10
2

μPD75216ACW-051 Block Diagram

CIRCUIT DESCRIPTION

Pin Function Table

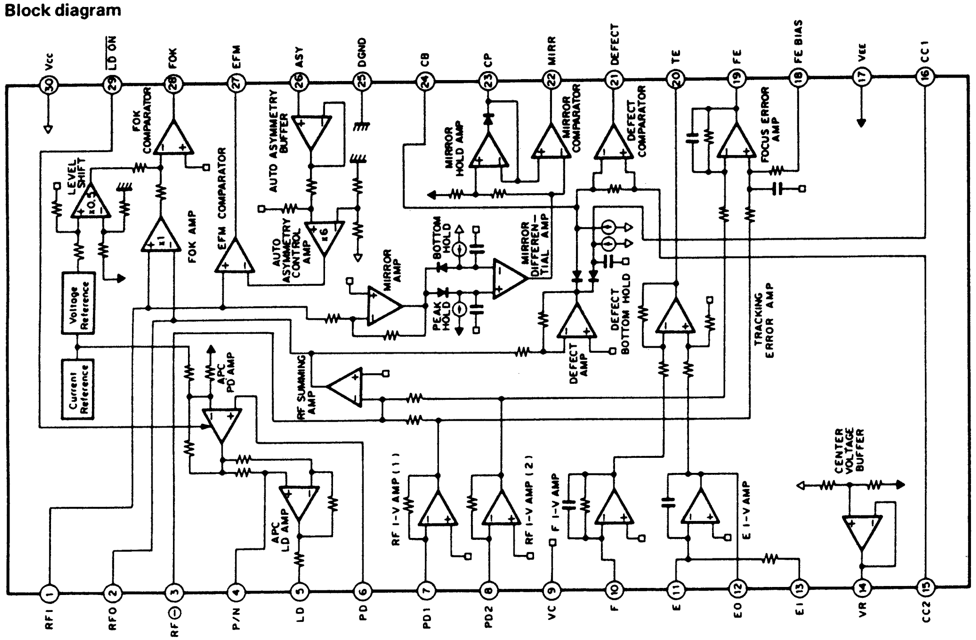
Pin No.	Symbol	I/O	Pin Name	Functions
1～4	S3～S0	O	Pd～Pa	FL display segment indication and key scan signal output
5	P00/INT4	I	SENSE	Sensing signal input (from CXD1125QZ, CXA1244S)
6	P01/$\overline{SCK}$	I	WFCK	Q data read-off clock input (from CXD1125QZ)
7	P02/SO	I	SUBQ	Q data input (from CXD1125QZ)
8	P03/SI	I	CRCF	Q data CRC OK ("H") input (from CXD1125QZ)
9	P10/INT0	I	RCI	Remote control signal input
10	P11/INT0	I	SCOR	Q data sync signal input (from CXD1125QZ)
11	P12/INT0	I	FOK	Focus OK ("H") input (from CXA1081M)
12	P13/TI0	I	GFS	EFM sync OK ("H") input (from CXD1125QZ)
13	P20	O	$\overline{RMUTE}$	Relay mute ON/OFF ("L"/"H")
14	P21	O	EMPH	Emphasis ON/OFF ("H"/"L")
15	P22	O	DIRC	DIRC signal output (to CXA1244S)
16	P23	O	MUTG	MUTG signal output; Mute ON/OFF ("H"/"L") (to CXD1125QZ)
17	P30	O	FGSW	Focus gain switch signal output
18	P31	I	$\overline{SLT\ SW}$	Start limit switch signal input (SW ON = "L")
19	P32	I	$\overline{OPN\ SW}$	Tray open switch signal input (SW ON = "L")
20	P33	I	$\overline{CLS\ SW}$	Tray close switch signal input (SW ON = "L")
21	P60	I	K1	Key input for front panel
22	P61	I	K2	
23	P62	I	K3	
24	P63	I	K4	
25	P40	O	DATA	Control data signal output (to CXD1125QZ, CXA1244S)
26	P41	O	XLT	Control data latch signal output (to CXD1125QZ, CXA1244S)
27	P42	O	CLK	Control data clock signal output (to CXD1125QZ, CXA1244S)
28	P43	O	LDC	Laser ON/OFF ("H"/"L") signal output
29	PPO	O	XRST	Control reset signal output (to CXD1125QZ, CXA1244S)
30	X1	I	X1	Clock input pin (1/2 clock of CXD1125QZ) (Oscillating frequency 4.2336 MHz)
31	X2	O	X2	
32	Vss	—	Vss	GND (ground)
35	P50	O	OPNM	Tray open/close signal output Normal (OPNM = "L", CLSM = "L") Open (OPNM = "H", CLSM = "L") Close (OPNM = "L", CLSM = "H")
36	P51	O	CLSM	
37	P52	O	VR_{DOWN}	Motor volume level down signal output
38	P53	O	VR_{UP}	Motor volume level up signal output
39	$\overline{RESET}$	I	$\overline{RESET}$	Reset signal input
40～53	T0～T13/PH0	O	G1～G14	FL display digit indication output
54	T14/S11	O	Pl	FL display segment indication output (Pt is also used for key scan)
55	T15/S10	O	Pk	
56	V_{LOAD}	I	V_{LOAD}	GND (ground)
57	V_{PRE}	I	V_{PRE}	GND (ground)
58～63	S9～S4	O	Pj～Pe	FL display segment indication and key scan signal output
64	V_{DD}	I	V_{DD}	+5 V power supply

RF amplifier CXA1081M (X29-1870-00 : IC1)

The CXA1081M supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator

Block diagram


Vcc
LD ON
FOK
EFM
ASY
DGND
CB
CP
MIRR
DEFECT
TE
FE
FE BIAS
VEE
CC1
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
LEVEL SHIFT
×0.5
FOK COMPARATOR
FOK AMP
×1
EFM COMPARATOR
AUTO ASYMMETRY BUFFER
AUTO ASYMMETRY CONTROL AMP
×6
MIRROR HOLD AMP
MIRROR COMPARATOR
DEFECT COMPARATOR
FOCUS ERROR AMP
BOTTOM HOLD
PEAK HOLD
MIRROR AMP
MIRROR DIFFERENTIAL AMP
DEFECT AMP
DEFECT BOTTOM HOLD
TRACKING ERROR AMP
Voltage Reference
Current Reference
APC PD AMP
RF SUMMING AMP
APC LD AMP
RF I-V AMP (1)
RF I-V AMP (2)
F I-V AMP
E I-V AMP
CENTER VOLTAGE BUFFER
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
RFI
RFO
RF⊖
P/N
LD
PD
PD1
PD2
VC
F
E
EO
EI
VR
CC2

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	RFI	I	Input pin of the C-coupled signal output from the RF summing amp.
2	RFO	O	Check point of eye pattern for the RF summing amp output pin.
3	RF ⊖	I	RF summing amp feedback input pin.
4	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
5	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	APC PD amp input pin. (DC voltage: open)
7	PD1	I	RF I—V amp (1) invert input pin. Current input by connecting to PIN diode A + C.
8	PD2	I	RF I—V amp (2) invert input pin. Current input by connecting to PIN diode B + D.
9	VC	—	Connected to GND when using a positive (+)/negative (—) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	F I—V amp invert input pin. Current input by connecting to PIN diode F.
11	E	I	E I—V amp invert input pin. Current input by connecting to PIN diode E.
12	EO	O	E I—V amp output pin.
13	EI	I	E I—V amp feedback input pin. For E I—V amp gain adjustment.
14	VR	O	DC voltage output pin of (Vcc + VEE)/2.
15	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
16	CC1	O	Defect bottom hold output pin.
17	VEE	—	Connected to the negative power supply when using a positive (+)/negative (—) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
19	FE	O	Focus error amp output pin.
20	TE	O	Tracking error amp output pin.
21	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10kΩ load).
22	MIRR	O	Mirror comparator output pin. (DC voltage: connected to a 10kΩ load).
23	CP	I	Mirror hold capacitor output pin. Mirror comparator non-invert input.
24	CB	I	Defect bottom hold capacitor connect pin.
25	DGND	—	Connected to GND when using a positive (+)/negative (—) dual-voltage power supply. Connected to GND (VEE) when using a single-voltage power supply.
26	ASY	I	Auto asymmetry control input pin.
27	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10kΩ load).
28	FOK	O	FOK comparator output pin. (DC voltage: connected to a 10kΩ load).
29	LD ON	I	LD ON/OFF select pin. (DC voltage: when LD ON).
30	Vcc	—	Positive power supply.

CIRCUIT DESCRIPTION

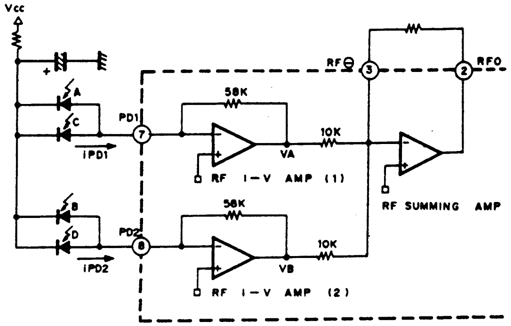
Explanation of function

- **RF amp**

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I–V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6k\Omega \times (i_{PD1} + i_{PD2})$$


Vcc
A
C
B
D
PD1
PD2
IPD1
IPD2
58K
10K
VA
VB
RF I–V AMP (1)
RF I–V AMP (2)
RF⊖
RFO
RF SUMMING AMP

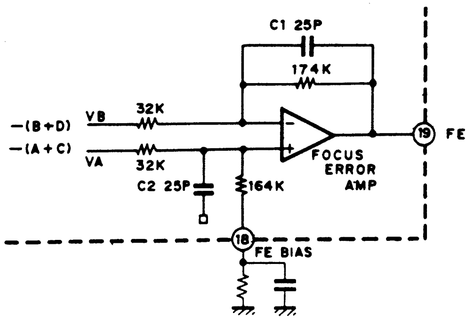
RF I–V amplifier

- **Focus error amp**

The difference between the RF I–V amp (1) output (VA) and the RF I–V amp (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4k\Omega$$


C1 25P
174K
–(B+D)
–(A+C)
VB
VA
32K
32K
C2 25P
164K
FOCUS ERROR AMP
FE
FE BIAS

CIRCUIT DESCRIPTION

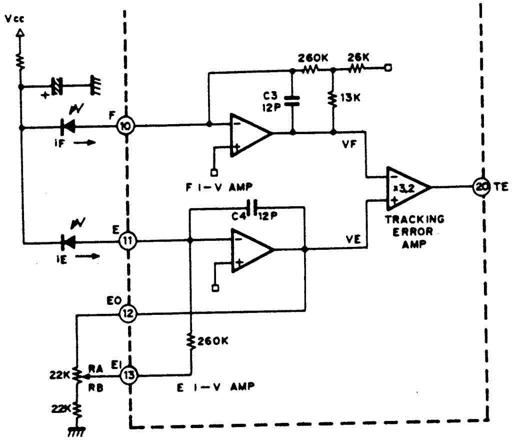
- **Tracking error amp**

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I–V amp and F I–V amp respectively. That is:

$$V_F = iF \times 403k\Omega$$
$$V_E = iE \times 260k\Omega \times R_A/(R_B + 22k) + (R_A + 260k)$$

The difference between the E I–V amp and the F I–V amp is calculated by the tracking error amp, and the photodiode (E–F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2$$
$$= (iE - iF) \times 1290k\Omega$$


Vcc
260K
26K
C3 12P
13K
F
IF
VF
F I–V AMP
×3.2
TE
TRACKING ERROR AMP
C4 12P
E
IE
VE
EO
EI
260K
22K
RA
RB
22K
E I–V AMP

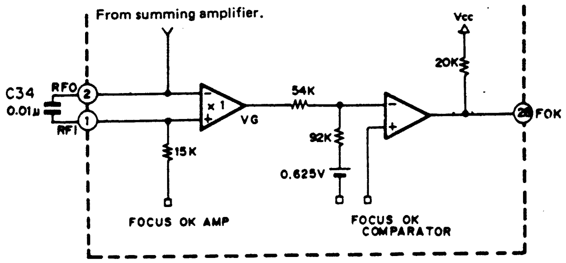
- **Focus OK circuit**

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RFI} - V_{RFO} \fallingdotseq -0.37V$.

C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C34 = 0.01μF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.


From summing amplifier.
C34 0.01μ
RFO
RFI
×1
VG
15K
FOCUS OK AMP
54K
92K
0.625V
Vcc
20K
FOK
FOCUS OK COMPARATOR

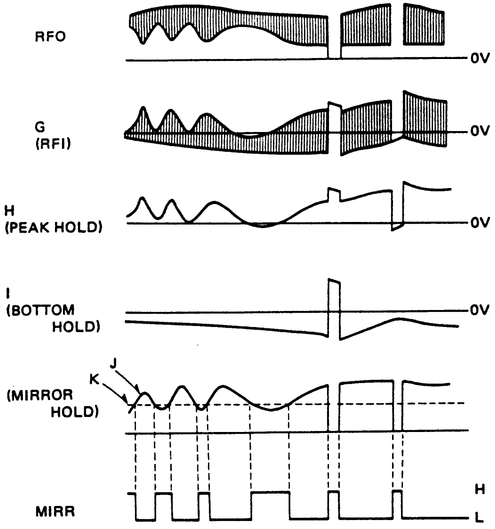
CIRCUIT DESCRIPTION

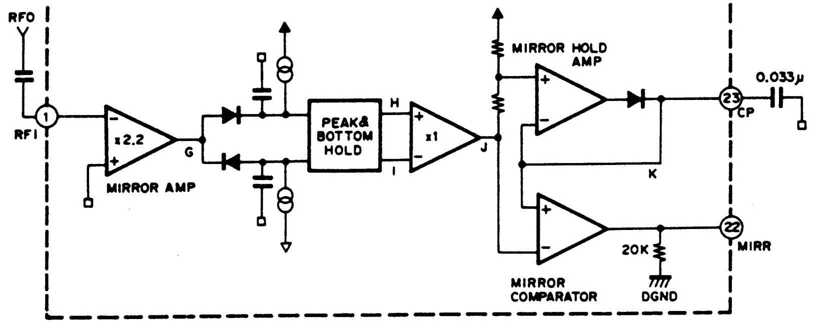
- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.


RFO
0V
G
(RFI)
0V
H
(PEAK HOLD)
0V
I
(BOTTOM
HOLD)
0V
J
K
(MIRROR
HOLD)
MIRR
H
L


RFO
RFI
1
x2.2
MIRROR AMP
G
PEAK&
BOTTOM
HOLD
H
I
x1
J
MIRROR HOLD
AMP
K
0.033μ
23
CP
22
MIRR
20K
MIRROR
COMPARATOR
DGND

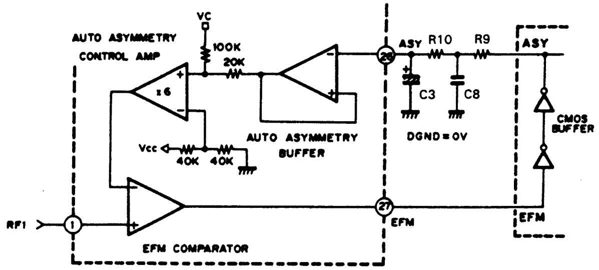
CIRCUIT DESCRIPTION

- **EFM comparator**

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

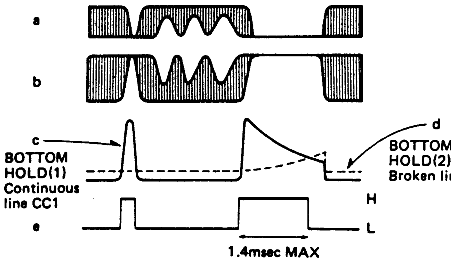
The EFM comparator is designed as a current switc type, and the "H" and "L" levels are not equal to power voltages. Therefore, feedback is required vi CMOS buffer.

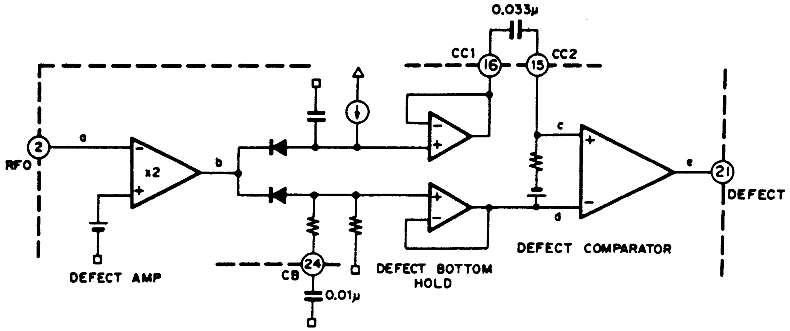
R9, R10, C3 and C8 constitute a LPF to obtain the component of (Vcc+DGND)/2 (V). If the cut-off freque (fc) is set to more than 500Hz, leakage of the EFM low quency signals will be greatly increased and will resu a degradation of the block error rate.


AUTO ASYMMETRY
CONTROL AMP
VC
100K
20K
x6
Vcc
40K
40K
AUTO ASYMMETRY
BUFFER
26
ASY
R10
R9
C3
C8
DGND=0V
ASY
CMOS
BUFFER
RFI
1
EFM COMPARATOR
27
EFM
EFM

- **Defect circuit**

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generates the mirror defect detecting signals.


a
b
c
BOTTOM
HOLD(1)
Continuous
line CC1
d
BOTTOM
HOLD(2)
Broken li
e
H
L
1.4msec MAX


0.033μ
CC1
16
15
CC2
RFO
2
a
x2
b
DEFECT AMP
c
d
e
21
DEFECT
DEFECT COMPARATOR
24
C8
0.01μ
DEFECT BOTTOM
HOLD

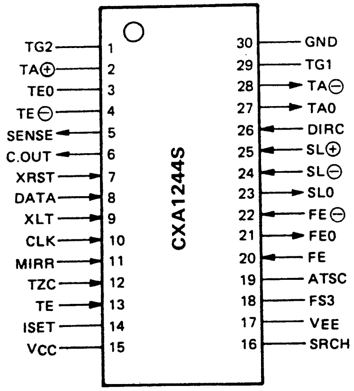
CIRCUIT DESCRIPTION

Servo signal processor CXA1244S (X32-1170-11: IC1)

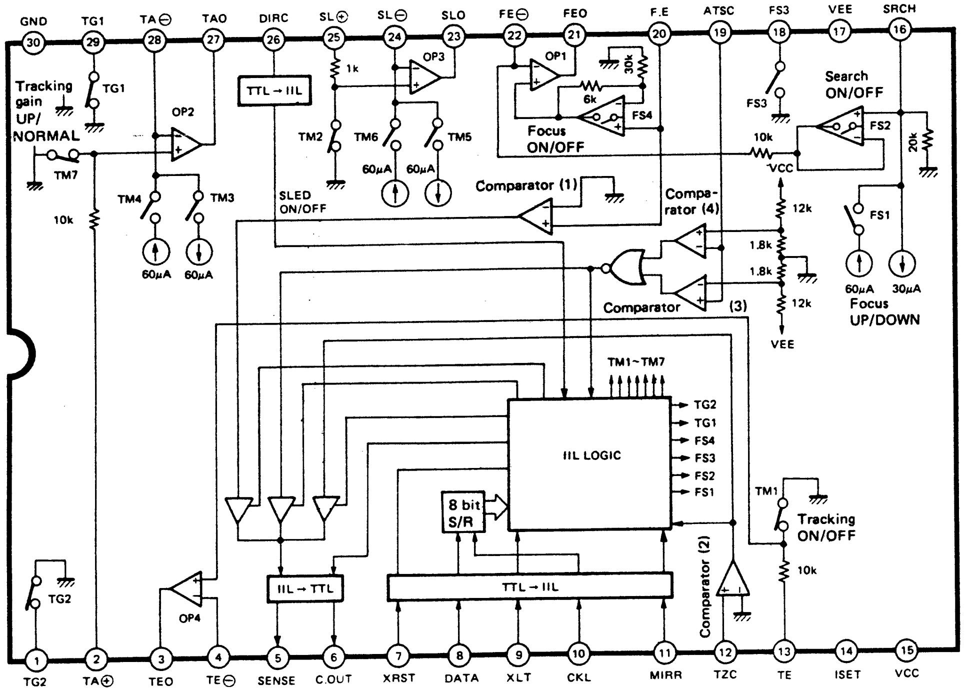
CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- ○Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- ○ Sled control (servo ON/OFF, fast forward, fast reverse)

Terminal connection diagram


TG2 1
TA⊕ 2
TEO 3
TE⊖ 4
SENSE 5
C.OUT 6
XRST 7
DATA 8
XLT 9
CLK 10
MIRR 11
TZC 12
TE 13
ISET 14
VCC 15
30 GND
29 TG1
28 TA⊖
27 TAO
26 DIRC
25 SL⊕
24 SL⊖
23 SLO
22 FE⊖
21 FEO
20 FE
19 ATSC
18 FS3
17 VEE
16 SRCH
CXA1244S

Block diagram


GND 30
TG1 29
TA⊖ 28
TAO 27
DIRC 26
SL⊕ 25
SL⊖ 24
SLO 23
FE⊖ 22
FEO 21
F.E 20
ATSC 19
FS3 18
VEE 17
SRCH 16
Tracking gain UP/NORMAL
TG1
TM7
OP2
10k
TM4
TM3
60μA
60μA
TTL→IIL
SLED ON/OFF
1k
OP3
TM2
TM6
TM5
60μA
60μA
OP1
30k
6k
FS4
Focus ON/OFF
Comparator (1)
Compa-rator (4)
Comparator
(3)
FS3
Search ON/OFF
FS2
20k
10k
VCC
12k
1.8k
1.8k
12k
VEE
FS1
60μA
30μA
Focus UP/DOWN
TM1~TM7
IIL LOGIC
TG2
TG1
FS4
FS3
FS2
FS1
8 bit S/R
TM1
Tracking ON/OFF
10k
Comparator (2)
OP4
TG2
IIL→TTL
TTL→IIL
1 TG2
2 TA⊕
3 TEO
4 TE⊖
5 SENSE
6 C.OUT
7 XRST
8 DATA
9 XLT
10 CKL
11 MIRR
12 TZC
13 TE
14 ISET
15 VCC

CIRCUIT DESCRIPTION

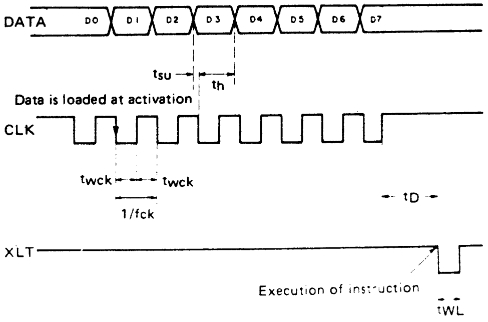
Explanation of terminals

Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TEO		Output of operational amplifier 4.
4	TE ⊖		Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally +5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally −5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a trakcing error is input through BPF. In this equipment it is connected to GND level and is not used.
20	FE	I	Input of focus error signal.
21	FEO	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SLO	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TAO	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus erro voltage is 0V or higher. Used at the time of FOCUS PULL operation.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%). But this is not used in this equipment.
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross. tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑ in FWD JUMP or on detection of TZC ↓ in REV JUMP

Note 2 : Digital unit timing chart


DATA
D0
D1
D2
D3
D4
D5
D6
D7
tsu
th
Data is loaded at activation
CLK
twck
twck
1/fck
tD
XLT
Execution of instruction
tWL

CIRCUIT DESCRIPTION

System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

Note : The antishock circuit is not used in this equipment.

CIRCUIT DESCRIPTION

Serial data truth value table

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

TRACKING CONTROL		D2 (Brake)	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

AS : ANTI SHOC

TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

DC : DIRC input terminal

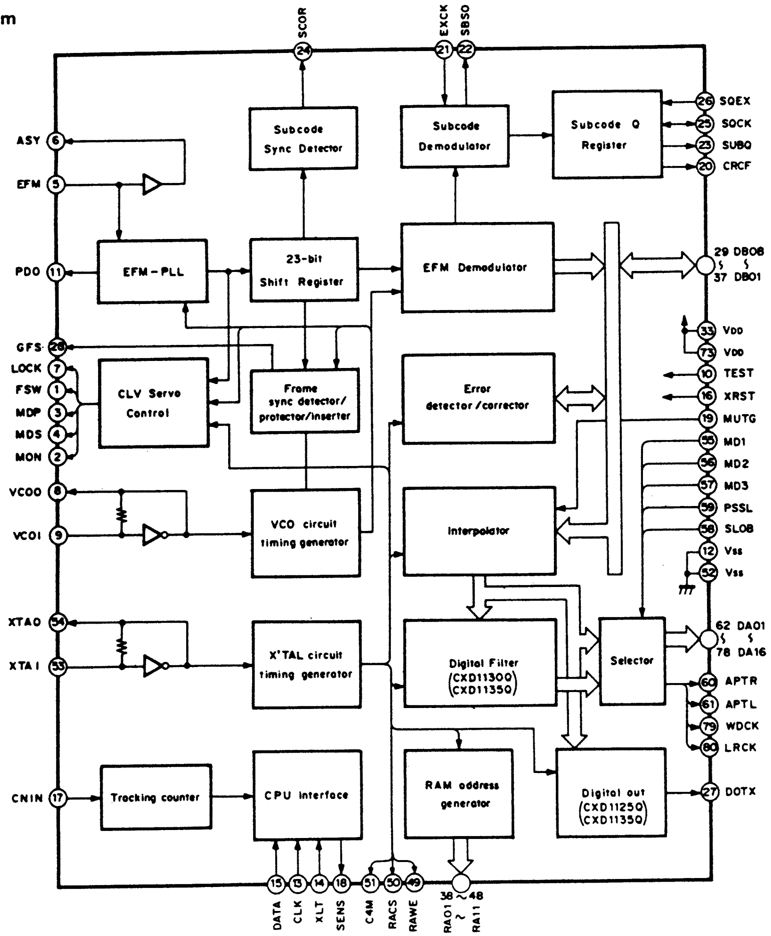
CIRCUIT DESCRIPTION

Digital signal processing LSI CXD1125QZ (X32-1170-11: IC6)

The CXD1125QZ is the digital signal processing LSI for the compact disc player, and has the following functions. All the digital signals for reproduction can be processed internally with this one-chip design.

- Bit clock reproduction by an EFM-PLL circuit.
- EFM data demodulation.
- Frame sync signal detection, protection and insertion.
- Powerful error detection and correction.
- Interpolation with average value or by holding the previous value.
- Demodulaiton of sub code signal or error detection of sub code Q.
- Spindle motor CLV servo.
- 8-bit tracking counter.
- CPU interface with a serial bus.
- Sub code Q register.
- D/A interface output.

Block diagram


SCOR
EXCK
SBSO
24
21
22
Subcode Sync Detector
Subcode Demodulator
Subcode Q Register
26 SQEX
25 SQCK
23 SUBQ
20 CRCF
ASY 6
EFM 5
PDO 11
EFM-PLL
23-bit Shift Register
EFM Demodulator
29 DB08 ~ 37 DB01
GFS 28
LOCK 7
FSW 1
MDP 3
MDS 4
MON 2
CLV Servo Control
Frame sync detector/protector/inserter
Error detector/corrector
33 VDD
73 VDD
10 TEST
16 XRST
19 MUTG
55 MD1
56 MD2
57 MD3
59 PSSL
58 SLOB
12 Vss
52 Vss
VCOO 8
VCOI 9
VCO circuit timing generator
Interpolator
XTAO 54
XTAI 53
X'TAL circuit timing generator
Digital Filter (CXD11300 / CXD11350)
Selector
62 DA01 ~ 78 DA16
60 APTR
61 APTL
79 WDCK
80 LRCK
CNIN 17
Tracking counter
CPU interface
RAM address generator
Digital out (CXD11250 / CXD11350)
27 DOTX
15 DATA
13 CLK
14 XLT
18 SENS
51 C4M
50 RACS
49 RAWE
38~48 RA01 ~ RA11

CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PD0	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	–	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L". normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code Q read-off clock.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + SI output.
25	WFCK	O	Write Frame Clock output. f = 7.35kHz when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	–	Power supply (+ 5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
51	C4M	O	Crystal dividing output. f = 4.2336MHz.
52	Vss	–	GND (0V).
53	XTAI	I	Crystal oscillator input. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select output. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	–	Power supply (+ 5V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C210}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C210 output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 88.2kHz.
80	LRCK	O	Strobe signal output. 44.1kHz.

Notes:

C1F1 : } Error correction status monitor output for C1 decode.
C1F2 :
C2F1 : } Error correction status monitor output for C2 decode.
C2F2 :
C2PO : C2 pointer signal.
C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.
RFCK : Read frame clock output. 7.35MHz when locked to the crystal line.
WFCK : Write frame clock output. 7.35MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to the EFM signal.
UGFS : Non-protected frame sync pattern output.
GTOP : Frame sync protect status display output.
RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.
C4LR : Strobe signal. 176.4kHz.
$\overline{\text{C210}}$: C210 invert output.
C210 : Bit clock output. 2.1168MHz.
DATA : Audio signal serial data output.

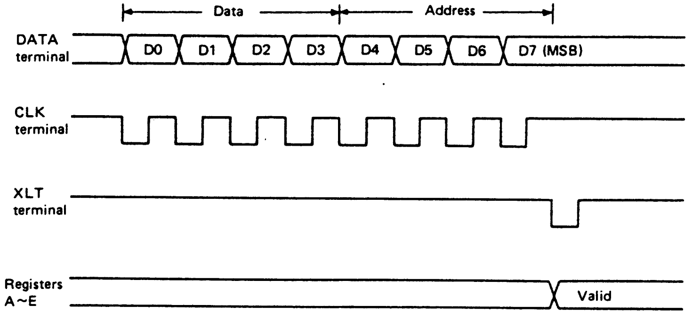
CIRCUIT DESCRIPTION

Explanation of functions

- **CPU interface**

1) Data input

Each register may be set by input of 4 bit address, and 4 bit data from LSB in the timing that is shown in Fig. 6–2 to three terminals, XLT, CLK and DATA. The addre and data of each terminal are as shown in Table 6–2, a their functions are as follows. The contents of each regist become entirely 0 when XRST = "L".



Timing chart for data input

2) Registers

○ Register 9 – New function control
Controls the new functions added to the CX23035.

D3 : ZCMT Switches the zero cross mute function ON/OFF. Details are described in **"Interpolation and Mute, Attenuate"**.

D2 : HZPD One of the defect countermeasures. Switches ON/OFF the function which makes the PD0 pin a high impedance (Z) for a maximum of 0.55ms from the rising edge of GFS. Details are described in **"Countermeasures to defects"**.

D1 : NCLV Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in **"CLV servo control"**.

D0 : CRCQ Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in **"5) Subcode output"**.

○ Register A – Sync. protection, attenuator control

D3 : GSEM ⎫
D2 : GSEL ⎬ Provided for switching frame synk. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of **"EFM demodulation"**.
D1 : WSEL ⎭
D0 : ATTM

D0 : ATTM Used for attenuating audio signals by 12dB, and the details will be described in the paragraph of **"D/A interface"**.

○ Registers B and C – Counter set, more significant 4 bits (register C) and less significant 4 bits (register B)

these registers are used for setting the tracking count value. the data of registers B and C are preset in the counter through the 4 bit buffer register assigned by address. Accordingly, when data of either register B or C is inp the contents of both registers are preset in the cour simultaneously as 8 bit data (either buffer register is "OLD" data.)

D3 : DIV The dividing ratio of RFCK and WFCK CLV-P mode is fixed, and the phase is co pared with RFCK/4 or WFCK/4 respectiv regardless of the status of D3, then out from the MDP pin.

○ Register D-CLV control

D3 : DIV Used for setting the frequency dividing ra of RFCK, WFCK in the CLV-P mode. Wh D3 = 0,, phase comparison of RFCK/4 a WFCK/4 is made, and when D3 = 1, ph comparison of RFCK/8 and WFCK/8 made, and output is made out of MDP t minal in each case.

D2 : T_B Used for determining the period of botto hold in the CLV-S and CLV-H modes.
Bottom hold is made in the period of RF /32 when D2 = 0 or in the period of RFC 16 when D2 = 1.

D1 : T_p Used for setting the period of peak hold the CLV-S mode. Peak hold is made in t period of RFCK/4 when D1 = 0 or in t period of RFCK/2 when D1 = 1.

D0 : GAIN Used for setting the gain of MDP termi output in the CLV-S and CLV-H mod It is −12dB (time of 3/4 out of the period RFCK/2 is of high impedance) when D0 = or is 0dB when D0 = 1.

○ Register E-CLV mode
It is as shown in Table 6–2.

The details of each mode will be described in the paragraph of CLV servo control.

Register name	Command	Address D7~D4	Data D3	Data D2	Data D1	Data D0	SENSE terminal
9*1	New function control	1 0 0 1	ZCMT	HZPD	NCLV	CRCQ	Z
A*2	Sync protection, attenuator control	1 0 1 0	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4 bits	1 0 1 1	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4 bits	1 1 0 0	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1 1 0 1	DIV	TB	TP	GAIN	Z
E*4	CLV mode	1 1 1 0		CLV mode			$\overline{\text{Pw} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDC pin is always active	PDC pin is "Z" at the trailing edge of GFS
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG terminal	dB
0	0	0
0	1	–∞
1	0	–12
1	1	–12

***3 Register D**

DIV	D3	0	RFCK/4 & WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 & WFCK/8	
TB	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	–12dB	Gain at MDP terminal in CLV-S, CLV-H mode
		1	0dB	

***4 Register E**

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0 0 0 0	L	Z	L	L
KICK	1 0 0 0	H	Z	L	H
BRAKE	1 0 1 0	L	Z	L	H
CLV-S	1 1 1 0	CLV-S	Z	L	H
CLV-H	1 1 0 0	CLV-H	Z	L	H
CLV-P	1 1 1 1	CLV-P	CLV-P	Z	H
CLV-A	0 1 1 0	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z : High impedance

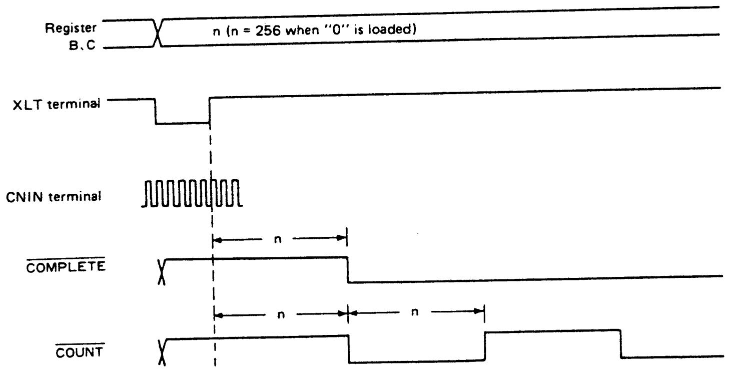
List of registers

3) Trakcing counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in register B and C. Count of CNIN pulses is started at raising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal ($\overline{\text{COMPLETE}}$) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENSE terminal. When the address is set at "C", signal ($\overline{\text{COUNT}}$) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 6–3.



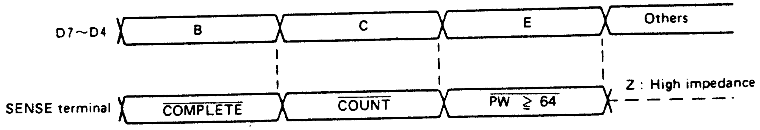
Tracking counter timing chart

4) SENSE

The following signals are output from SENSE terminal depending on the address of D7~D4.

1. $\overline{\text{COMPLETE}}$: Address is "B"; Shown in Fig. 6–3.
2. $\overline{\text{COUNT}}$: Address is "C"; Shown in Fig. 6–3.
3. $\overline{\text{PW} \geqq 64}$: Address is "E"; this signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note : Address setting is determined only by the data that corresponds to D4~D7 which can be input from DATA terminal shown in Fig. 6–2.



Timing chart of SENSE terminal

5) Sub code output

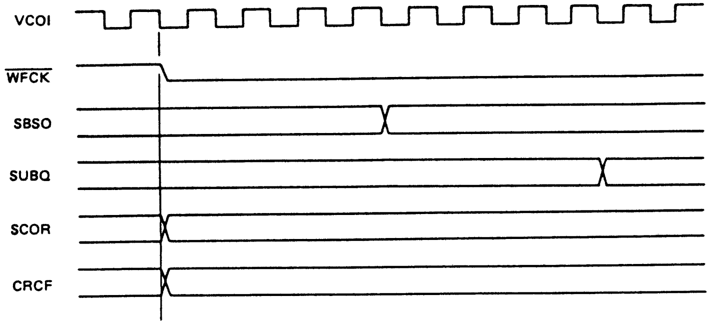
Sub codes P~W loaded in the 8 bit shift register are output out of SBSO terminal in accordance with the clock input through EXCK terminal. when SCOR terminal is "H", S0 · S1 signal is output.

Sub code Q is as follows, depending on the SQEX pin status.

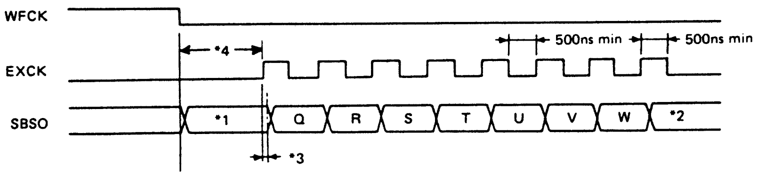
(i) When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The WFCK is also output from the SQCK pin.

(ii) When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4 bits, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4 bits of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF


VCOI
WFCK
SBSO
SUBQ
SCOR
CRCF

(b) Timing of SBSO, EXCK

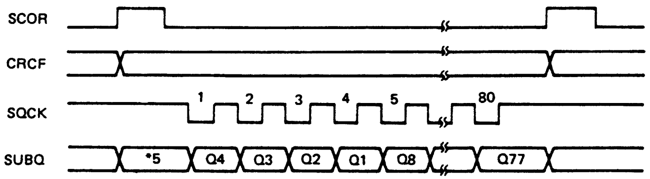

WFCK
EXCK
SBSO
*4
500ns min
500ns min
*1
Q
R
S
T
U
V
W
*2
*3

*1 : Sub code P is output when SCOR is 0.
S0 · S1 is output when SCOR is 1.
*2 : SBSO is 0 when 8 or more pulses are input to EXCK.
*3 : 4T ~ 6T if the period of VCO is expressed as T.
*4 : Make EXCK low for 10μs from the rising edge of WFCK.
One time period of T = 8.6436MHz.

(1) Timing chart of sub code outputs

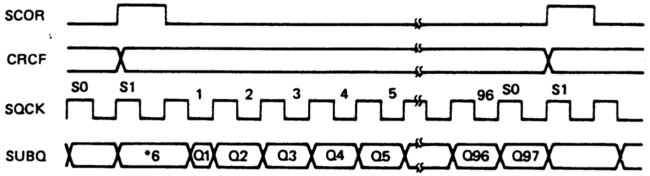
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX= "H" level


SCOR
CRCF
SQCK
1
2
3
4
5
80
SUBQ
*5
Q4
Q3
Q2
Q1
Q8
Q77

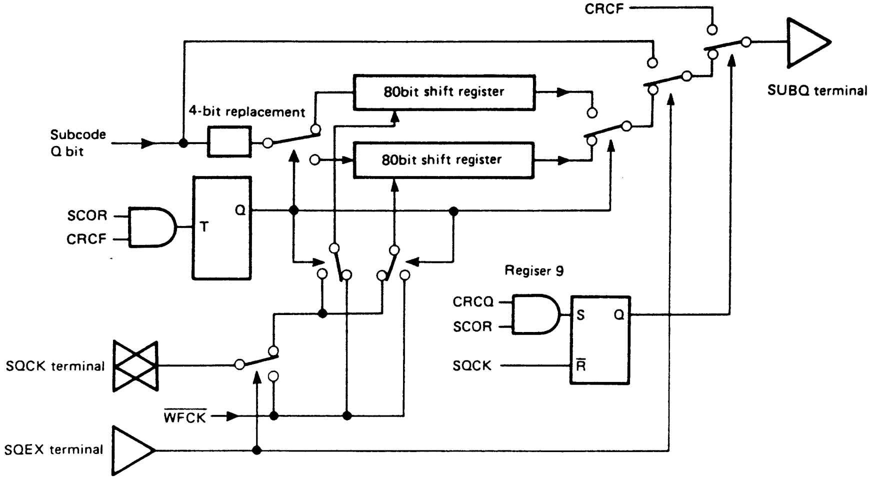
*5 : CRCF when CRCQ flag is "1", undefined when "0".

SQEX= "L" level


SCOR
CRCF
SQCK
S0
S1
1
2
3
4
5
96
S0
S1
SUBQ
*6
Q1
Q2
Q3
Q4
Q5
Q96
Q97

*6 : CRCF when CRCQ flag is "1", Q98,Q1 when "0".

(2) Timing chart of sub code outputs


CRCF
SUBQ terminal
80bit shift register
4-bit replacement
Subcode Q bit
80bit shift register
SCOR
CRCF
T
Q
Regiser 9
CRCQ
SCOR
S
Q
SQCK
R
SQCK terminal
WFCK
SQEX terminal

• EFM demodulation

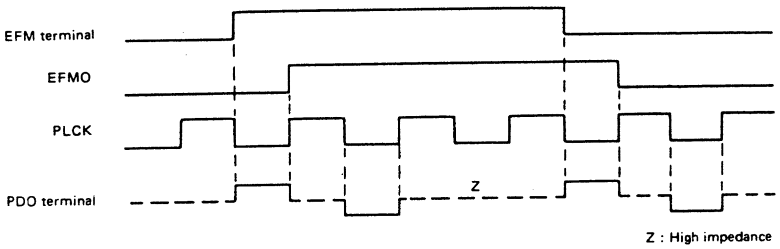
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32MHz synchronized with this clock by the EFM-PLL circuit.

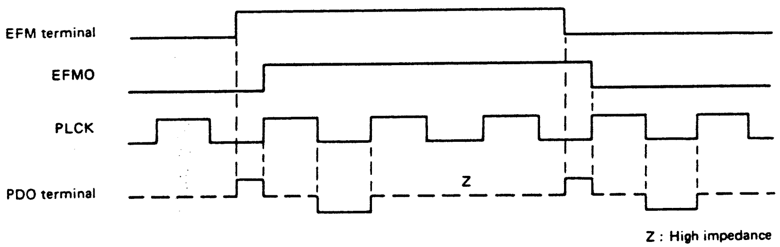
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO terminal. The mean value of PDO terminal is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM terminal, EFMO, PLCK and PDO are shown in Fig. 6–7.

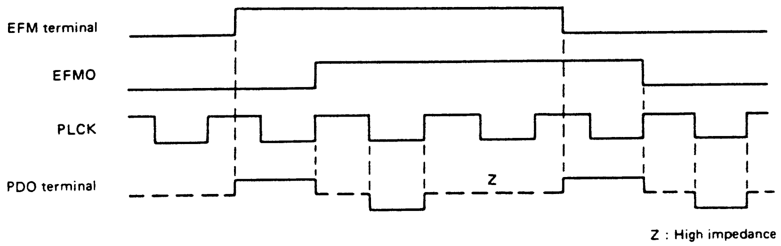
(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal



Timing charts of EFM-PLL circuit

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23 bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL. If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218MHz/588 = 7.35kHz)

A 4 bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4 bit counter is reset with the next frame synchronizing signal. the GTOP terminal is of "H" while this operation is performed. Further, GFS terminal is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the wondow is output out of UGFS (DA05 terminal at the time when PSSL = L.)

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frames to be interpolated	UGFS (PSSL = "L")
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14 bit data is taken out of the 23 bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08~DB01) terminals) of the RAM in accordance with the OENB signal transmitted from said block.

• Sub code demodulation

1) Sub code demodulation

synchronizing signals S0, S1 of 14 bit sub codes are detected out of the 23 bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR terminal and S0 · S1 is output out of SBSO terminal (only when SCOR = H.)

Data (P~W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ terminal, and at the same time, it is loaded in the 8 bit shift register and is output out of SBSO terminal in correspondence to a clock from EXCK terminal.

The detials of this timing will be shown in the paragraph of CPU interface.

2) Sub code Q error detection

The CRC sub code result is output from the CRCF pin in synchronism with the SCOR pin. It goes "L" when an error is detected. At the same time as the CRCQ flag is "1", the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detialed in **"CPU interface"**.

- **RAM interface (generation of external RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block, the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal. This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'Tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block. This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock C212 (8.4672MHz/4). The data output out of the RAM is C2 pointer first, less significant 8 bits out of 16 bits and finally more significant 8 bits.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data. In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8 bit data directed to the RAM interface block from the error correction block. The requests from the error correction unit are of the lowest priority among requests of three types. After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal. This block generates the address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing. This interleave processing is subjected to data lag by the unit of a frame. Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer. The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   - The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Pointe R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum. In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are not accepted in this timing. When requests 2, 3 are generated simultaneously, priority is given to request 2, and if a requestis generated during execution of either request, priority is given to the job in execution.

6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synmchronized with the clock of X'Tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter. As a result, there is no case where data without error correction is output to the D/A.

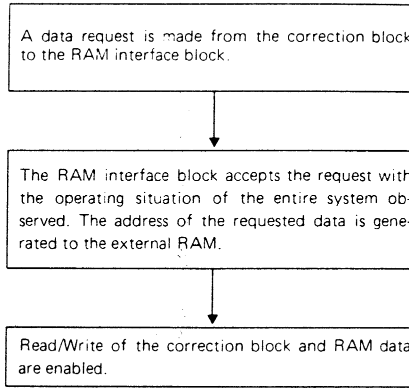
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

- **Error correction**

1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16k RAM stores these pointer data in addition to audio data.
3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bits).
6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" when a period of minimum 472ns after deactivation of terminal RFCK. C2FL is the AND of C2F1 and C2F2.

Note : 472ns : One period of 2.1168MHz

8) The flow of data with the external RAM is as foll



A data request is made from the correction block to the RAM interface block.

The RAM interface block accepts the request with the operating situation of the entire system observed. The address of the requested data is generated to the external RAM.

Read/Write of the correction block and RAM data are enabled.

9) When PSSL is set at "L", a signal that is capabl monitoring error correction is output. C1F1, C C2F2 output to DA01~DA04 are these monitor sig This signal is reset to "L" when a period of minir 472 ns has elapsed since deactivation of RFCK.

The levels and meanings of these signals at the tim deactivaiton of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
0	1	Double error correctior
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No Error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

CIRCUIT DESCRIPTION

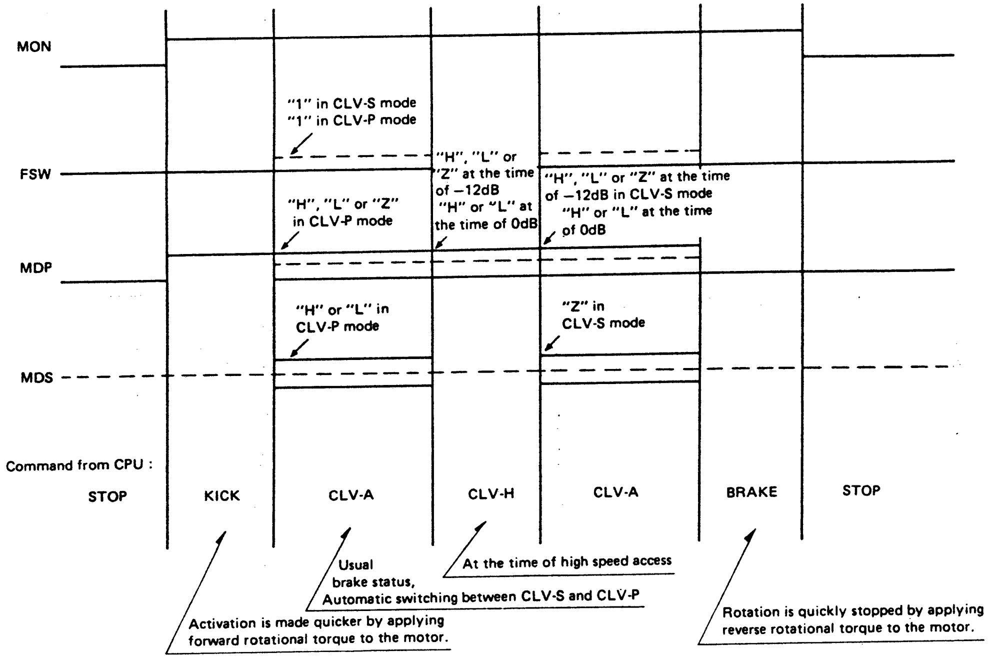
- **CLV servo control**

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

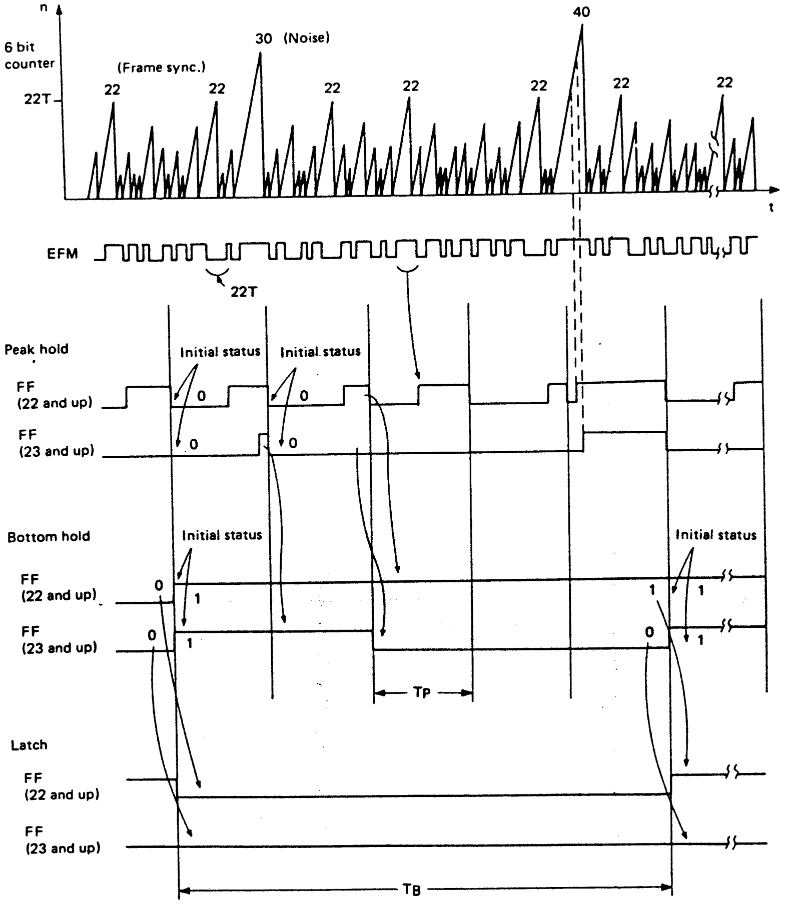

MON
FSW
MDP
MDS
Command from CPU :
STOP
KICK
CLV-A
CLV-H
CLV-A
BRAKE
STOP
"1" in CLV-S mode
"1" in CLV-P mode
"H", "L" or "Z" in CLV-P mode
"H", "L" or "Z" at the time of −12dB "H" or "L" at the time of 0dB
"H", "L" or "Z" at the time of −12dB in CLV-S mode "H" or "L" at the time of 0dB
"H" or "L" in CLV-P mode
"Z" in CLV-S mode
Usual brake status, Automatic switching between CLV-S and CLV-P
At the time of high speed access
Activation is made quicker by applying forward rotational torque to the motor.
Rotation is quickly stopped by applying reverse rotational torque to the motor.

Z : High impedance

Typical control of spindle motor

CIRCUIT DESCRIPTION

TP : RFCK/2 or RFCK/4 in the case of CLV-S,
F8M/256 in the case of CLV-H
TB : RFCK/16 or RFCK/32 in the case of
CLV-S, CLV-H


n
6 bit counter
22T
(Frame sync.)
22
22
30 (Noise)
22
22
22
40
22
22
t
EFM
22T
Peak hold
Initial status
Initial status
FF (22 and up)
FF (23 and up)
0
0
0
0
Bottom hold
Initial status
Initial status
FF (22 and up)
FF (23 and up)
0
1
0
1
1
1
0
1
TP
Latch
FF (22 and up)
FF (23 and up)
TB

Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

4) CLV-S : Register E = 1100'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practive, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more.

Either 0dB or 12dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

5) CLV-P: Register E = 1111'B

PLL servo mode.

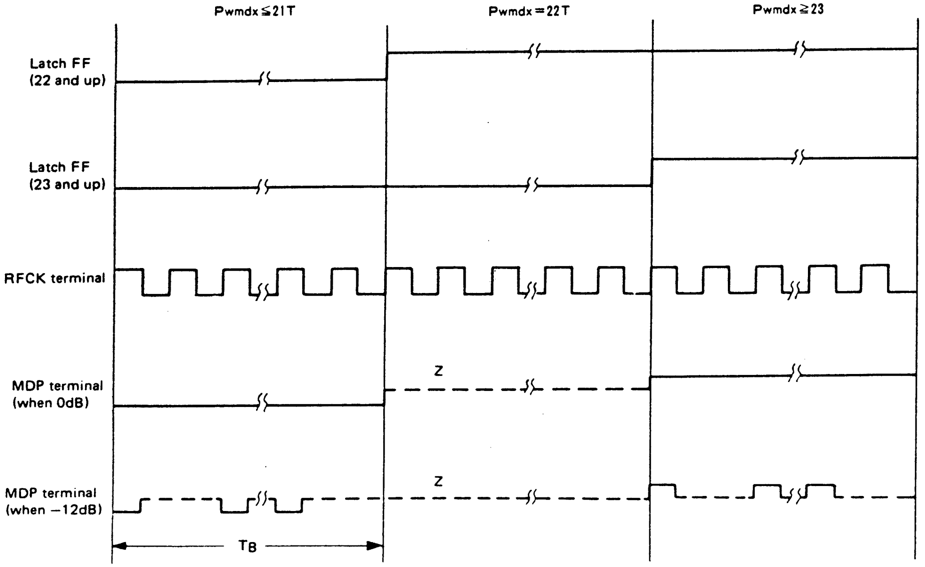
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized. If the 8.4672/2MHz period is T, and the time when WFCK is "H" is tHW, then the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (tHW–279T) X 32, and then goes "L" until the next trailing edge of WFCK.

MDS ≦ "H" when tHW = 279T,

MDS = "L" when tHW ≧ 279T.

The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ tHW ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when tHW = 288T, a 7.35kHz signal, with a duty cycle of 50% is output.

FSW = "Z", MON = "H".


Pwmdx≦21T
Pwmdx=22T
Pwmdx≧23
Latch FF (22 and up)
Latch FF (23 and up)
RFCK terminal
MDP terminal (when 0dB)
MDP terminal (when −12dB)
Z
Z
TB

Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

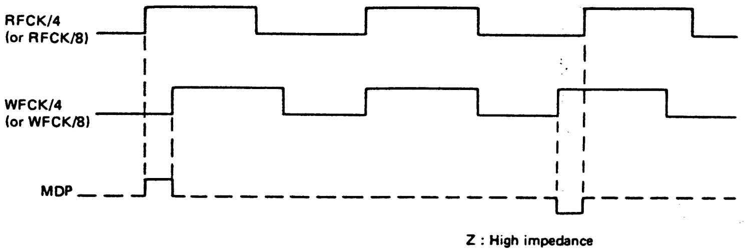
6) CLV-P : Register E = 1111'B

PLL servo mode.

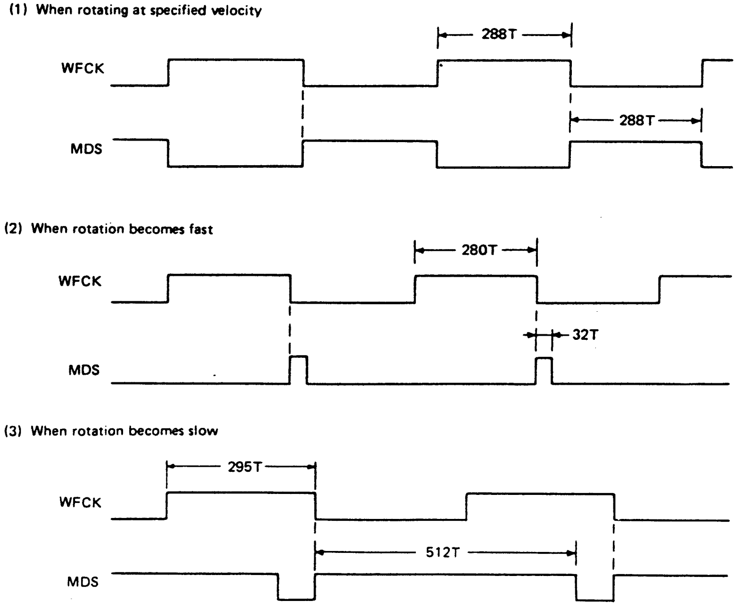
Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of 8.4672/2MHz is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW–279T)

x 32 with 7.35kHz as a period and that is
curing the remaining time is produced ou
MDS terminal. MDS = "L" when tHW ≦ 27
MDS = "H" when tHW ≦ 297T. When 280T
tHW ≦ 296T, the MDS terminal change
32T steps from 32T to 544T. When sync
nized, for instance, that is, when tHW = 28
a signal of 7.35kHz of DUTY 50% is produ
FSW = "Z", MON = "H".

MDP terminal


RFCK/4 (or RFCK/8)
WFCK/4 (or WFCK/8)
MDP
Z : High impedance

MDS terminal (The Period of 4.2336MHz is expressed as "T".)


(1) When rotating at specified velocity
288T
WFCK
288T
MDS
(2) When rotation becomes fast
280T
WFCK
32T
MDS
(3) When rotation becomes slow
295T
WFCK
512T
MDS

Timing chart in CLV-P mode

7) CLV-A: Register E = 0110'B
The mode used for normal play status.
The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and insertion block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode. When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is perfomred in register E. The description of these registers are detialed in **"CPU interface"**.
Note: When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

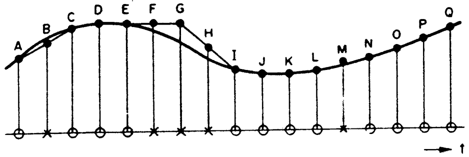
8) CLV-A' : Register E = 0101'B
New auto servo mode added to the CX23035. The difference between CLV-A. and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.
The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

- **Interpolation and D/A converter interface**

1) Interpolation circuit block

3 byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8 bits and more significant 8 bits. The total 16 bits constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16 bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O : Without C2 pointer
X : With C2 pointer

Mean value interpolation

$$B=\frac{1}{2}(A+C)$$

$$H=\frac{1}{2}(E+I)$$: When pointers are continuous

$$M=\frac{1}{2}(L+N)$$

Previous value hold

$$F=G=E$$

16 bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H". C2PO signal outputs C2 pointer to the 16 bit data directed to DA01–DA16 (PSSL = H), DA16 (PSSL = L). In other words, it means that the 16 bit data that is output when C2PO is "H" is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute (– ∞ dB) or attenuate (–12dB) the audio signal in accordance with the MUTG terminal and ATTM signal of the CPU interface block.

ATTM	MUTG	Attenuation value	Remarks
0	0	0dB	
1	0	–12dB	
0	1	– ∞ dB	See Note
1	1	–12dB	See Note

NOTE : When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter is loaded.

- **Mode setting**

The various kinds of mode can be set by combining the following pins. (Refer to the table below.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input terminal					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

(Note)
- 8M/16M : Selection of clock, XTAL or XTAO. 8.4672MHz/16.9344MHz
- DO OFF/ON : Digital out OFF/ON
- DF OFF/ON : Digital filter OFF/ON
- P/S : Parallel output/serial output
- OB/2's : Offset binary/2's complement
- CD ROM/AUDIO : Compatible to CD ROM/Compatible to audio

1) Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344MHz and 8.4672MHz. However, when digital out is used, the clock must be set to 16.9344MHz.

2) Selection of digital out (Refer to "D/A interface")

When digital out is set to ON, a signal conforming to the D/A interface format is output from the DOTX pin. When it is set to OFF, the DCTX pin outputs the WFCK signal. In the DP-969, this function is fixed to ON.

3) Selection of digital filter

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

4) Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data. When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

DA01 → C1F1 : } Error correction status monitor
DA02 → C1F2 : } output at C1 decode.
DA03 → C2F1 : } Error correction status monitor
DA04 → C2F2 : } output at C2 decode.
DA05 → C2FL : Correction status output, C2FL = C2F1·C2F2.
DA06 → C2PO : C2 pointer signal.
DA07 → RFCK : Read frame clock signal, 7.35kHz when locked to the crystal line.
DA08 → WFCK : Write frame clock signal, 7.35kHz when locked.
DA09 → $\overline{\text{PLCK}}$: 1/2 of the divided signal from the VCO pin, 4.3218MHz when locked.
DA10 → UGFS : Non-protect frame sync signal.
DA11 → GTOP: Frame sync protect status display signal.
DA12 → RAOV : Jitter margin over or underflow display signal.
DA13 → C4LR : 4 times the LRCK signal.
DA14 → $\overline{\text{C210}}$: Bit clock (invert signal of C210).
DA15 → C210 : Internal system clock (4.2336MHz when DF is ON, 2.1168MHz when CXD1125Q or DF is OFF).
DA16 → DATA : Serial data output (MSB or LSB first output).

5) Selection of OFFSET BINARY/2'S COMPLEMENT

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

6) Selection of CD ROM/AUDIO compatibility

When MD1 = MD2 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8 bits of the 16 bits, only the C2 pointer corresponding to the upper 8 bits goes "H", and the lower 8 bits are processed as the correct data.

- **D/A Interface**

The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

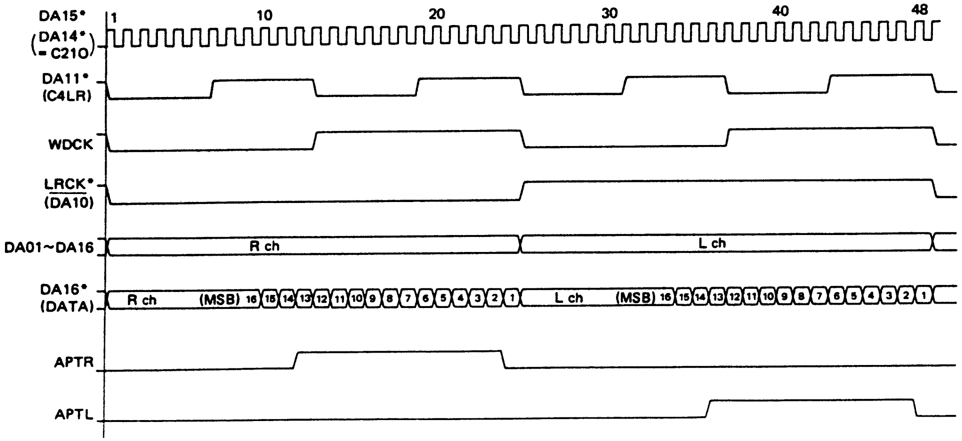
- **Countermeasures to defect**

To counter a defect, the PDC pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after approx. 0.55ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

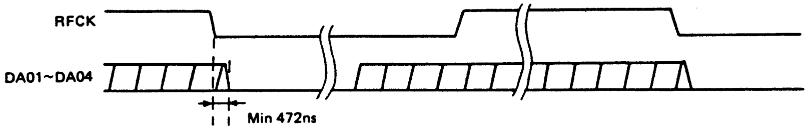
This operation is similar to that for the FSW pin. However, while the FSW outputs a fixed signal when not in CLV-A' mode, the LOCK pin always output the above signal.

- **Timing chart**

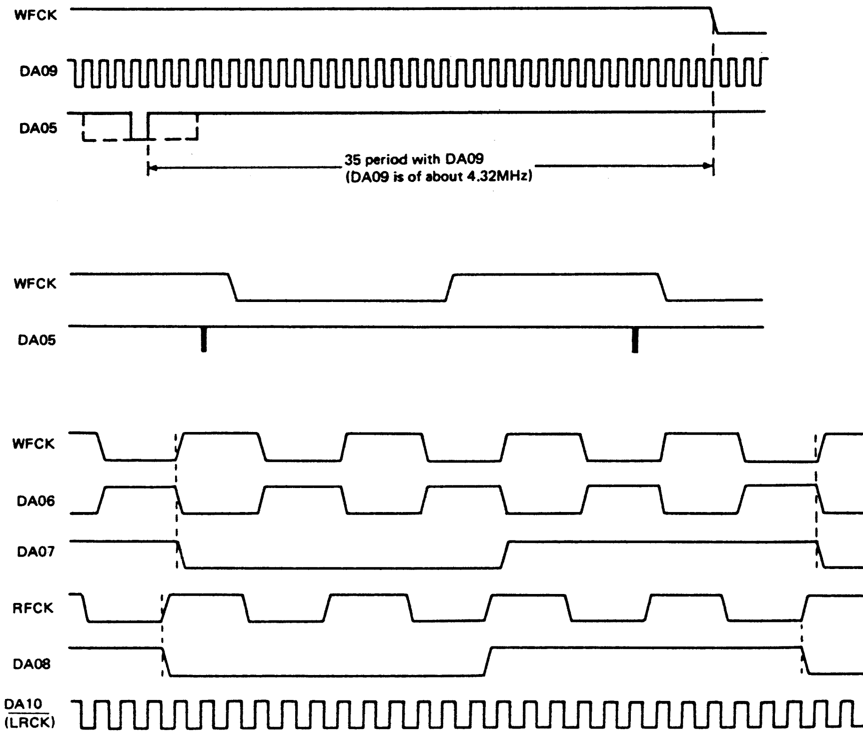

DA15*
(DA14* = C210)
1
10
20
30
40
48
DA11* (C4LR)
WDCK
LRCK* (DA10)
DA01~DA16
R ch
L ch
DA16* (DATA)
R ch (MSB) 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
L ch (MSB) 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
APTR
APTL

*PSSL = "L"

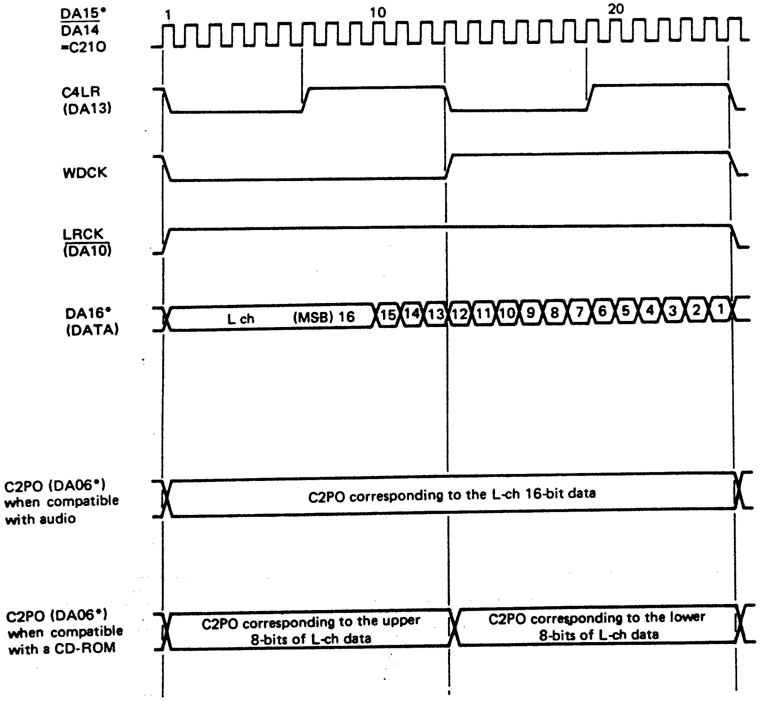
Timing chart of audio output


RFCK
DA01~DA04
Min 472ns

- DA01~DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
- ANDing signal of C2F1 and C2F2 is output out of C2FL termnal.

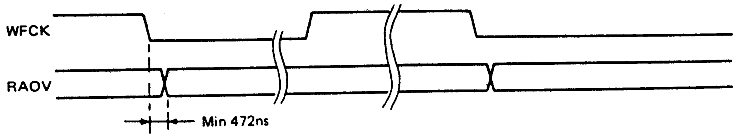

WFCK
DA09
DA05
35 period with DA09
(DA09 is of about 4.32MHz)
WFCK
DA05
WFCK
DA06
DA07
RFCK
DA08
DA10 (LRCK)

Timing chart of DA01~DA16 output when PSSL="L"


DA15*
DA14
=C210
1
10
20
C4LR
(DA13)
WDCK
LRCK
(DA10)
DA16*
(DATA)
L ch
(MSB) 16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
C2PO (DA06*)
when compatible
with audio
C2PO corresponding to the L-ch 16-bit data
C2PO (DA06*)
when compatible
with a CD-ROM
C2PO corresponding to the upper
8-bits of L-ch data
C2PO corresponding to the lower
8-bits of L-ch data

Timing chart of C2PO output (when PSSL="L")

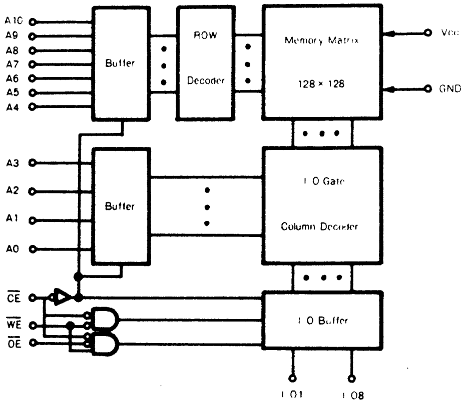
* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.


WFCK
RAOV
Min 472ns

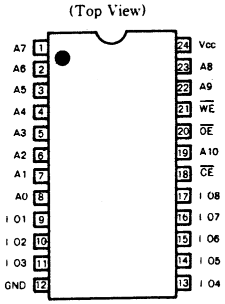
Timing chart of RAOV output

Static RAM CXK5816SP-12L
(X32-1170-11: IC7)

Block Diagram


A10
A9
A8
A7
A6
A5
A4
Buffer
ROW
Decoder
Memory Matrix
128 × 128
Vcc
GND
A3
A2
A1
A0
Buffer
I O Gate
Column Decoder
CE
WE
OE
I O Buffer
I 01
I 08

Terminal connection diagram


(Top View)
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
I 01 9
I 02 10
I 03 11
GND 12
24 Vcc
23 A8
22 A9
21 WE
20 OE
19 A10
18 CE
17 I 08
16 I 07
15 I 06
14 I 05
13 I 04

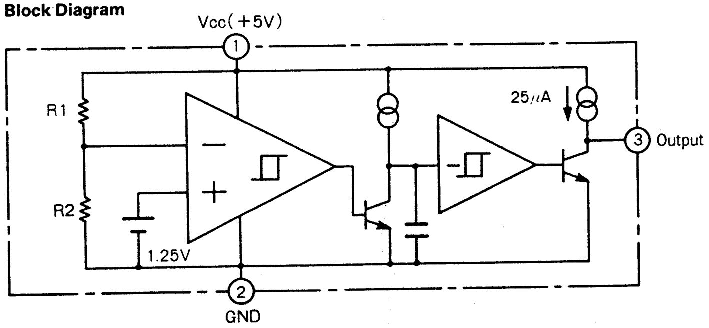
Explanation of terminals

Terminal name	Function
A0～A10	Address input
I/01～I/08	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Outfit enable input
Vcc	+5V
END	Ground

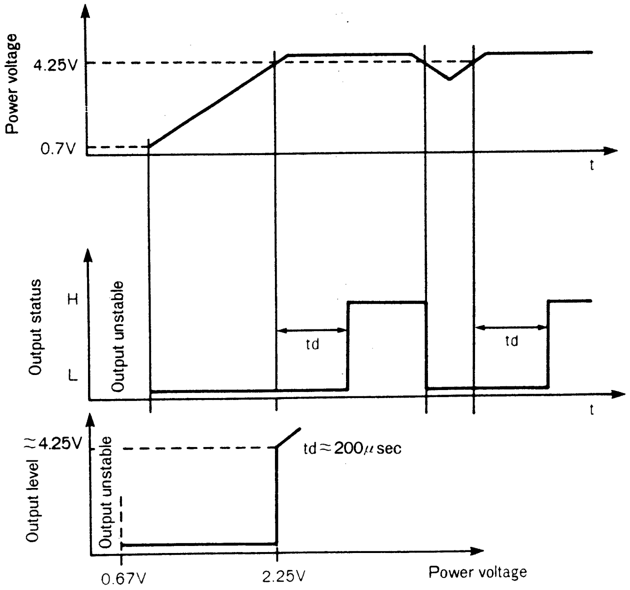
CIRCUIT DESCRIPTION

Reset IC: M51951ASL (X32-1170-11: IC11)

Block Diagram


Vcc(+5V)
1
R1
R2
1.25V
25μA
3
Output
2
GND

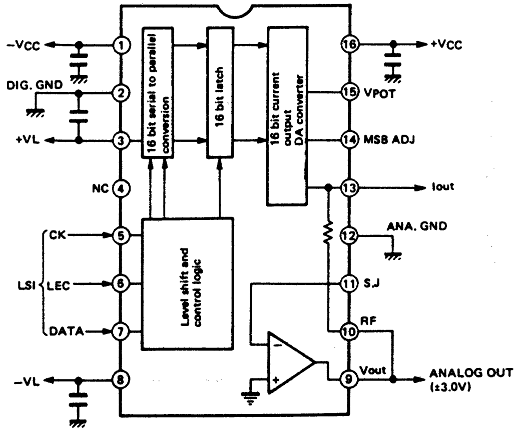
Operating Waveform



CIRCUIT DESCRIPTION

DA Converter: PCM56P-K (X25-3050-XX: IC1, IC2)

Block diagram/
Terminal connection diagram


–Vcc
DIG. GND
+VL
NC
CK
LSI
LEC
DATA
–VL
1
2
3
4
5
6
7
8
16 bit serial to parallel conversion
16 bit latch
16 bit current output DA converter
Level shift and control logic
16
15
14
13
12
11
10
9
+Vcc
VPOT
MSB ADJ
Iout
ANA. GND
S.J
RF
Vout
ANALOG OUT
(±3.0V)

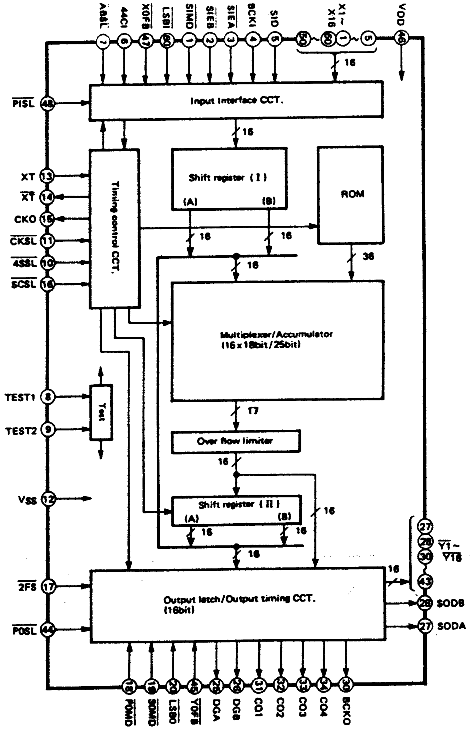
Explanation of terminals

Terminal No.	Terminal name	Function	Terminal No.	Terminal name	Function
1	–Vcc	Analog negative power supply.	9	Vout	Voltage output
2	DIG GND	Digital ground.	10	RF	Feedback resistor.
3	+VL	Logic positive power supply.	11	S.J	Summing junction (op amp. input).
4	NC	No connection.	12	ANA GND	Analog ground.
5	CK	Clock input.	13	Iout	Current output.
6	LEC	Latch enable control input.	14	MSB ADJ	MSB adjustment terminal.
7	DATA	Data input.	15	V POT	Potentiometer terminal.
8	–VL	Logic negative power supply	16	+Vcc	Analog positive power supply.

CIRCUIT DESCRIPTION

Digital filter: SM5804D (X25-3050-XX: IC14)

Block diagram


$\overline{\mathrm{ABSL}}$ 7
44CI 6
$\overline{\mathrm{XOFB}}$ 47
$\overline{\mathrm{LSBI}}$ 60
$\overline{\mathrm{SIMD}}$ 1
$\overline{\mathrm{SIEB}}$ 2
$\overline{\mathrm{SIEA}}$ 3
BCKI 4
SID 5
X1 ~ X16 50 ~ 60 1 ~ 5
VDD 46
16
$\overline{\mathrm{PISL}}$ 48
Input Interface CCT.
XT 13
$\overline{\mathrm{XT}}$ 14
CKO 15
$\overline{\mathrm{CKSL}}$ 11
$\overline{\mathrm{4SSL}}$ 10
$\overline{\mathrm{SCSL}}$ 16
Timing control CCT.
Shift register (I)
(A)
(B)
ROM
36
Multiplexer/Accumulator (16x18bit/25bit)
17
Over flow limiter
TEST1 8
TEST2 9
Test
Vss 12
Shift register (II)
27 28 30 ~ 43 $\overline{\mathrm{Y1}}$ ~ $\overline{\mathrm{Y16}}$
$\overline{\mathrm{2FS}}$ 17
$\overline{\mathrm{POSL}}$ 44
Output latch/Output timing CCT. (16bit)
28 SODB
27 SODA
18 $\overline{\mathrm{POMD}}$
19 $\overline{\mathrm{SOMD}}$
20 $\overline{\mathrm{LSBO}}$
45 $\overline{\mathrm{YOFB}}$
25 DGA
26 DGB
31 CO1
32 CO2
33 CO3
34 CO4
30 BCKO

CIRCUIT DESCRIPTION

Explanation of Pins

With this LSI, the switching between the serial and parallel inputs/outputs is performed by the $\overline{\mathrm{PISL}}$ and $\overline{\mathrm{POSL}}$ pins. Some of the functions of pins X1 to X16 and $\overline{\mathrm{Y1}}$ to $\overline{\mathrm{Y16}}$ may be changed by this switching.

All the terminals of this unit function with $\overline{\mathrm{PISL}}$ = H.

Note: ip designates an input jack with a pull-up resistor.

Pin No.	$\overline{\mathrm{PISL}}$ = H		$\overline{\mathrm{PISL}}$ = L		Function
	Pin Name	I/O	Pin Name	I/O	
1	$\overline{\mathrm{SIMD}}$	ip			Serial input mode switching.
			X5	ip	Parallel data input (Bit 5).
2	$\overline{\mathrm{SIEB}}$	ip			B CH serial input enable.
			X4	ip	Parallel data input (Bit 4).
3	$\overline{\mathrm{SIEA}}$	ip			A CH serial input enable.
			X3	ip	Parallel data input (Bit 3).
4	BCKI	ip			Serial input bit clock input.
			X2	ip	Parallel data input (Bit 2).
5	SID	ip			Serial input data.
			X1	ip	Parallel data input (LSB).
6	44CI	ip	←	ip	44.1 kHz sync clock input.
7	$\overline{\mathrm{ABSL}}$	ip	←	ip	$\overline{\mathrm{ABSL}}$ = H → 44 CI clock, H/L = A CH/B CH. $\overline{\mathrm{ABSL}}$ = L → 44 CI clock, H/L = B CH/A CH.
8	TEST 1	ip	←	ip	Test input 1 (Normally Open).
9	TEST 2	ip	←	ip	Test input 2 (Normally Open).
10	$\overline{\mathrm{4SSL}}$	ip	←	ip	Normally $\overline{\mathrm{4SSL}}$ = H or Open. $\overline{\mathrm{4SSL}}$ = L when input is 16.9344 MHz or 17.2872 MHz.
11	$\overline{\mathrm{CKSL}}$	ip	←	ip	$\overline{\mathrm{CKSL}}$ = H → External clock input. $\overline{\mathrm{CKSL}}$ = L → X'tal oscillation.
12	Vss		←		GND power supply pin (0 V).
13	XT	I	←	I	$\overline{\mathrm{CKSL}}$ = H → Clock input. $\overline{\mathrm{CKSL}}$ = L → X'tal oscillation input.
14	$\overline{\mathrm{XT}}$	O	←	O	$\overline{\mathrm{CKSL}}$ = H → (Open). $\overline{\mathrm{CKSL}}$ = L → X'tal oscillation output.
15	CKO	O	←	O	Clock output.
16	$\overline{\mathrm{SCSL}}$	ip	←	ip	System clock 96 fs → $\overline{\mathrm{SCSL}}$ = H. System clock 98 fs → $\overline{\mathrm{SCSL}}$ = L.
17	$\overline{\mathrm{2FS}}$	ip	←	ip	Open.
18	$\overline{\mathrm{POMD}}$	ip	←	ip	$\overline{\mathrm{POMD}}$ = H → Normal parallel output mode. $\overline{\mathrm{POMD}}$ = L → In-phase parallel output mode.
19	$\overline{\mathrm{SOMD}}$	ip	←	ip	$\overline{\mathrm{SOMD}}$ = L with serial output.
20	$\overline{\mathrm{LSBO}}$	ip	←	ip	$\overline{\mathrm{LSBO}}$ = H → MSB-first serial output. $\overline{\mathrm{LSBO}}$ = L → LSB-first serial output.
21	(NC)		←		(NC)
22	(NC)		←		(NC)
23	(NC)		←		(NC)
24	(NC)		←		(NC)
25	DGA	O	←	O	A CH deglitch control output.
26	DGB	O	←	O	B CH deglitch control output.
27	SODA	O			A CH serial data output.
			$\overline{\mathrm{Y1}}$	O	Parallel output (inverted, LSB).

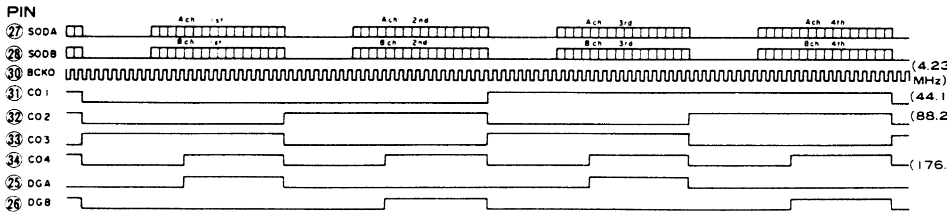
CIRCUIT DESCRIPTION

Pin No.	$\overline{PISL}$ = H		$\overline{PISL}$ = L		Function
	Pin Name	I/O	Pin Name	I/O	
28	SODB	O			B CH serial data output.
			$\overline{Y2}$	O	Parallel output (inverted, Bit 2).
29	(NC)		←		Internally short-circuited to VDD. Not to be connected externally.
30	BCKO	O			Serial output bit clock output.
			$\overline{Y3}$	O	Parallel output (inverted, Bit 3).
31	CO1	O			Serial output control clock 1.
			$\overline{Y4}$	O	Parallel output (inverted, Bit 4).
32	CO2	O			Serial output control clock 2.
			$\overline{Y5}$	O	Parallel output (inverted, Bit 5).
33	CO3	O			Serial output control clock 3.
			$\overline{Y6}$	O	Parallel output (inverted, Bit 6).
34	CO4	O			Serial output control clock 4.
			$\overline{Y7}$	O	Parallel output (inverted, Bit 7).
35	(NC)	Hz			(NC)
			$\overline{Y8}$	O	Parallel output (inverted, Bit 8).
36	(NC)	Hz			(NC)
			$\overline{Y9}$	O	Parallel output (inverted, Bit 9).
37	(NC)	Hz			(NC)
			$\overline{Y10}$	O	Parallel output (inverted, Bit 10).
38	(NC)	Hz			(NC)
			$\overline{Y11}$	O	Parallel output (inverted, Bit 11).
39	(NC)	Hz			(NC)
			$\overline{Y12}$	O	Parallel output (inverted, Bit 12).
40	(NC)	Hz			(NC)
			$\overline{Y13}$	O	Parallel output (inverted, Bit 13).
41	(NC)	Hz			(NC)
			$\overline{Y14}$	O	Parallel output (inverted, Bit 14).
42	(NC)	Hz			(NC)
			$\overline{Y15}$	O	Parallel output (inverted, Bit 15).
43	(NC)	Hz			(NC)
			$\overline{Y16}$	O	Parallel output (inverted, MSB).
44	$\overline{POSL}$	ip	←	ip	$\overline{POSL}$ = H→Serial output system. $\overline{POSL}$ = L→Parallel output system.
45	$\overline{YOFB}$	ip	←	ip	$\overline{YOFB}$ = H→2's complement display output. $\overline{YOFB}$ = L→Offset binary display output.
46	VDD		←		+ ve power supply pin (5 V).
47	$\overline{XOFB}$	ip	←	ip	$\overline{XOFB}$ = H→2's complement display input. $\overline{XOFB}$ = L→Offset binary display input.
48	$\overline{PISL}$	ip	←	ip	$\overline{PISL}$ = H→Serial input system. $\overline{PISL}$ = L→Parallel input system.
49	(NC)		←		(NC)

CIRCUIT DESCRIPTION

Pin No.	$\overline{PISL}$ = H		$\overline{PISL}$ = L		Function
	Pin Name	I/O	Pin Name	I/O	
50	(NC)	ip			(NC)
			X16	ip	Parallel data input (MSB).
51	(NC)	ip			(NC)
			X15	ip	Parallel data input (Bit 15).
52	(NC)	ip			(NC)
			X14	ip	Parallel data input (Bit 14).
53	(NC)	ip			(NC)
			X13	ip	Parallel data input (Bit 13).
54	(NC)	ip			(NC)
			X12	ip	Parallel data input (Bit 12).
55	(NC)	ip			(NC)
			X11	ip	Parallel data input (Bit 11).
56	(NC)	ip			(NC)
			X10	ip	Parallel data input (Bit 10).
57	(NC)	ip			(NC)
			X9	ip	Parallel data input (Bit 9).
58	(NC)	ip			(NC)
			X8	ip	Parallel data input (Bit 8).
59	(NC)	ip			(NC)
			X7	ip	Parallel data input (Bit 7).
60	$\overline{LSBI}$	ip			$\overline{LSBI}$ = H→MSB-first serial input. $\overline{LSBI}$ = L→LSB-first serial input.
			X6	ip	Parallel data input (Bit 6).

Serial Output Timing ($\overline{SOMD}$ = L, $\overline{SCSL}$ = H, system clock = 4.2336 MHz)

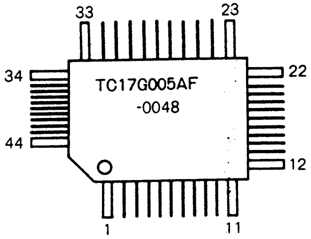


D/A distortion correct TC17G005AF-0048 (X25-3050-XX: IC15)

Explanation of terminals

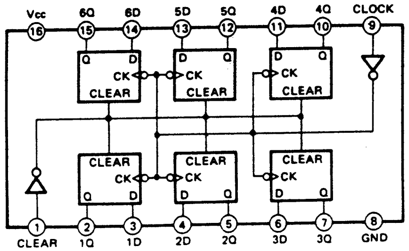
Terminal No.	Terminal name	I/O	Function
1	DLD	O	Lch data output
3	Lch	O	Lch D/A distortion correct output
4	Vss	—	GND
5	BCKD	O	Clock output
7	LRD	O	Latch enable control output
8	Vss	—	GND
9	Rch	O	Rch D/A distortion correct output
11	DRD	O	Rch data output
14	XT10	O	Crystal oscillator input terminal (16.934MHz)
15	XT11	I	
17	VDD	—	+5V
28	Vss	—	GND
39	VDD	—	+5V
40	LR	I	LRCK input (4fs)
41	BCK	I	BCK input (4fs)
42	DR	I	Rch data input
43	DL	I	Lch data input

Terminal connection diagram


33
23
34
22
TC17G005AF
-0048
44
12
1
11

Hexa D Flip-flop TC74HC174F (X25-3040-01: IC2)

Block diagram

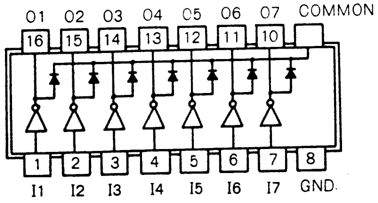

Vcc
6Q
6D
5D
5Q
4D
4Q
CLOCK
16
15
14
13
12
11
10
9
Q
D
CK
CLEAR
D
Q
CK
CLEAR
D
Q
CK
CLEAR
CLEAR
CK
Q
D
CLEAR
CK
D
Q
CLEAR
CK
D
Q
1
2
3
4
5
6
7
8
CLEAR
1Q
1D
2D
2Q
3D
3Q
GND

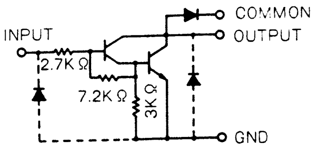
Truth table

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Transistor array (X25-3040-01: IC3) TD62003AP DARLINGTON DRIVER

Pin configuration


O1
O2
O3
O4
O5
O6
O7
COMMON
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
I1
I2
I3
I4
I5
I6
I7
GND


COMMON
OUTPUT
INPUT
2.7K Ω
7.2K Ω
3K Ω
GND

µPD4053BC 2-channel analog switch IC (X32-1170-11: IC2)

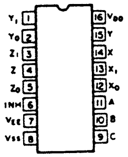
The µPD4053BC is a multiplexer composed of a level converter and analog SWs. The switches corresponding to the required channels are turned on according to the digital signal input to the control terminals.

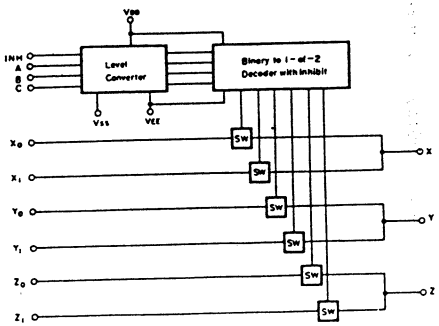
Truth table

Control input				"ON" channel
INHIBIT	C*	B	A	
L	L	L	L	Z_0、Y_0、X_0
L	L	L	H	Z_0、Y_0、X_1
L	L	H	L	Z_0、Y_1、X_0
L	L	H	H	Z_0、Y_1、X_1
L	H	L	L	Z_1、Y_0、X_0
L	H	L	H	Z_1、Y_0、X_1
L	H	H	L	Z_1、Y_1、X_0
L	H	H	H	Z_1、Y_1、X_1
H	×	×	×	NONE

H: "H" level, L: "L" level, X: H or L

Block diagram


Y1
Y0
Z1
Z
Z0
INH
VEE
VSS
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VDD
Y
X
X1
X0
A
B
C


VDD
INH
A
B
C
Level Converter
Binary to 1-of-2 Decoder with Inhibit
VSS
VEE
SW
X0
X1
Y0
Y1
Z0
Z1
X
Y
Z

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	–	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn power on to enter the Test mode. Press the REPEAT key, the tray opens and the LD emits light.	–	When the power is from 0.15 to0.4 mW, RF level is 1.0Vp-p or more, TE (servo open) is 2.0Vp-p or more and the diffraction grating is aligned correctly, the pickup is acceptable.	(a)
2	LASER PICKUP OPERATING CURRENT (Only when the pickup seems defective.)	–	Connect a DC ammeter across CN2 pin 6 and the pattern. (X32-1170)	Short-circuit pins TEST and turn power on to enter the Test mode. Press the REPEAT key, the tray opens and the LD emits light.	–	+5.5mA current value labeld on the laser pickup. If current is 40mA or more over the above value, it's defective.	(b)
3	VCO	–	Connect a frequency counter to CN11(PLCK) (X32-1170)	Turn Power OFF, then ON again. Stop mode	L9 (X32-1170)	4.27MHz	(c)
4	DIFFRACTION GRATING	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK key and confirm that the display is " 03oo".	–	Check that the diffraction grating is aligned correctly. (The grating cannot be adjusted.)	(d)
5	TRACKING ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK key and confirm that the display is " 03oo".	TE.BALANCE VR3 (X29-1870)	Symmetry between upper and lower patterns, or DC=0±0.05V	(e)
6	FOCUS ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Press the PLAY key, and confirm that the display is" 05oo".	FE BALANCE VR4 (X29-1870)	Optimum eye pattern	(f)
7	FOCUS GAIN	Test disc Type 4 Apply 900Hz, 40mVrms signal to CN3 pin 2 of PC board X32-1170	Use a servo jig, or connect a 47kΩ, 470pF LPF to pin 1 of CN3. (X32-1170)	Turn Power OFF then ON again, and press the PLAY key.	FOCUS GAIN VR1 (X29-1870)	40mVrms	(g)
8	TRACKING GAIN	Test disc Type 4 Apply 900Hz, 40mVrms signal to CN3 pin 4 of PC board X32-1170	Use a servo jig, or connect a 47kΩ, 470pF LPF to pin 5 of CN3. (X32-1170)	PLAY	TRACKING GAIN VR2 (X29-1870)	40mVrms	(g)
9	DAC OUTPUT	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 1kHz, 0dB signal in track No.2.	VR1: L VR2: R (X25-3050)	1.9~2.0Vrms	(h)
10	DAC DISTORTION	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 1kHz, -20dB signal in track No.15.	VR3: L VR4: R (X25-3050)	Minimum distortion	(h)
11	DAC DISTORTION	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 100Hz, 0dB signal in track No.4.	VR5: L VR6: R (X25-3050)	Minimum distortion	(h)

(Note) Type 4 disk: SONY YEDS-18 Test Disk or equivalent.

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche REPEAT, le plateau s'ouvre et le LD émet de la lumiére.	–	Quand l'alimentation est de 0,15 à0,4 mW le niveau RF de 1,0Vc-c ou plus, TE (asservissement ouvert) de 2,0Vc-c ou plus et le réseau de diffraction aligné correctement, le capteur est acceptable.	(a)
2	Courant de fonctionnement du capteur laser (Uniquement quand le capteur semble défectif.)	–	Raccorder un ampèremètre CC en travers de la broche 6 de CN2 et la forme. (X32-1170)	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche REPEAT, le plateau s'ouvre et le LD émet de la lumiére.	–	+ 5,5mA de valeur de courant indiquée sur le capteur laser. Si le courant est de 40mA ou bien supérieur à la valeur ci-dessus, il est défectif.	(b)
3	VCO	–	Raccorder un compteur de fréquence à CN11(PLCK). (X32-1170)	Couper l'alimentation, puis la redonner. Mode d'arrêt	L9 (X32-1170)	4,27MHz	(c)
4	RESEAU DE DIFFRACTION	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est " 03oo ".	–	Vérifier que le réseau de diffraction est correctement aligné. (Le réseau ne peut pas être ajusté.)	(d)
5	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est " 03oo "	TE BALANCE VR3 (X29-1870)	Symétrie entre les formes supérieure et inférieure ou DC = 0±0,05V	(e)
6	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Presser la touche PLAY et s'assurer que l'affichage est " 05oo "	FE BALANCE VR4 (X29-1870)	Forme optimum	(f)
7	GAIN DE MISE AU POINT	Disque test Type 4 Appliguer un signal 900Hz, 40mVrms à la troche 2 de CN3 sur la plaquette X32-1170.	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 1 de CN3.	Couper l'alimentation et la redonner puis presser la touch PLAY.	GAIN DE MISE AU POINT VR1 (X29-1870)	40mVrms	(g)
8	GAIN D'ALIGNEMENT	Disque test Type 4 Appliguer un signal 900Hz, 40mVrms à la troche 4 de CN3 sur la plaquette X32-1170.	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 5 de CN3.	PLAY	GAIN D'ALIGNEMENT VR2 (X29-1870)	40mVrms	(g)
9	SORTIE DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 1kHz, 0dB dans la piste n° 2.	VR1: G VR2: D (X25-3050)	1,9~2,0Vrms	(h)
10	DISTORSION DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 1kHz, -20dB dans la piste n° 15.	VR3: G VR4: D (X25-3050)	Distortion minimum	(h)
11	DISTORTION DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 100Hz, 0dB dans la piste n° 4.	VR5: G VR6: D (X25-3050)	Distortion minimum	(h)

(Remarque)Disque de type 4:Disque test SONY YEDS 18 ou équivalent.

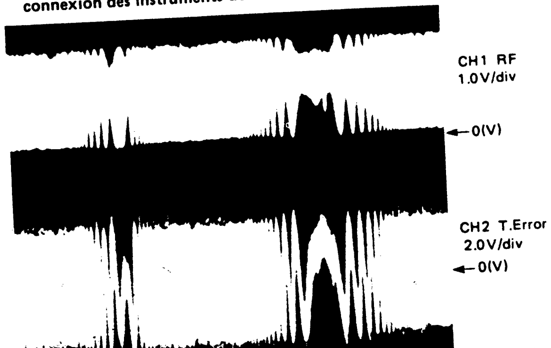
ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUN	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste REPEAT drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	–	Wenn bei einer Spannung von 0,15 bis 0,4 mW der RF-Pegel 1,0Vs-s oder mehr, TE (Servo-Offen) 2,0Vs-s beträgt und das Beugungsgitter richtig ausgerichtet ist, ist der Abtaster in Ordnung.	(a)
2	BETRIEBSSTROM DES LASERTONABNEHMERS (Nur wenn der Tonabnehmer defekt zu sein scheint)	–	Ein-Gleichstrom-Amperemeter zwischen CN2 Stift 6 und dem Muster anschließen. (X32-1170)	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste REPEAT drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	–	Stromwert + 5,5mA auf dem Lasertonabnehmer markiert. Wenn der Strom 40mA oder mehr über dem obigen Wert liegt, ist er defekt.	(b)
3	VCO	–	Einen Frequenzzähler an CN11(PLCK) anschließen. (X32-1170)	Die Spannungsversorgung aus-und dann wieder einschalten. Stop-Betriebsart	L9 (X32-1170)	4,27MHz	(c)
4	OPTISCHES GITTER	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß " 03oo " auf dem Display angezeigt wird.	–	Prüfen, ob das Beugungsgitter richtig ausgerichtet ist.(Das Gitter kann nicht eingestellt werden.)	(d)
5	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß " 03oo " auf dem Display angezeigt wird.	TE BALANCE VR3 (X29-1870)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC=0±0,05V	(e)
6	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oazilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Die PLAY-Taste drücken und prüfen, daß " 05oo " auf dem Display angezeigt wird.	FOKUS-FEHLERAUSGLEICH VR4 (X29-1870)	Optimales Augenmuster	(f)
7	FOKUSVERSTÄRKUNG	Testdisc Type 4 Ein 900Hz, 40mVrms Signal an Stift 2 von CN3 an platine X32-1170 anlegen.	Eine Servo-Lehre verwenden oder ein 47kΩ, 470pF Tiefpaßfilter an Stift 1 von CN3 anschließen.	Die Spannungsversorgung aus-und dann wieder einschalten, dann die PLAY-Taste drücken.	FOKUSVERSTÄRKUNG VR1 (X29-1870)	40mVrms	(g)
8	SPURHALTE-VERSTÄRKUNG	Testdisc Type 4 Ein 900Hz, 40mVrms Signal an Stift 4 von CN3 an platine X32-1170 anlegen.	Eine Servo-Lehre verwenden oder ein 47kΩ, 470pF Tiefpaßfilter an Stift 5 von CN3 anschließen.	PLAY	SPUHALTE-VERSTÄRKUNG VR2 (X29-1870)	40mVrms	(g)
9	DAC-AUSGANG	Testdisc. Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, 0dB Signal in Titel Nr. 2 wiedergeben.	VR1: L VR2: R (X29-1870)	1,9～2,0Vrms	(h)
10	DAC-VERZERRUNG	Testdisc Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, -20dB Signal in Titel Nr. 15 wiedergeben.	VR3: L VR4: R (X29-1870)	Minimale Verzerrung	(h)
11	DAC-VERZERRUNG	Testdisc Type 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 100Hz, 0dB Signal in Titel Nr. 4 wiedergeben.	VR5: L VR6: R (X29-1870)	Minimale Verzerrung	(h)

(Hinweis) Typ 4 Disc: SONY YEDS 18 Testdisc oder Äquivalent.

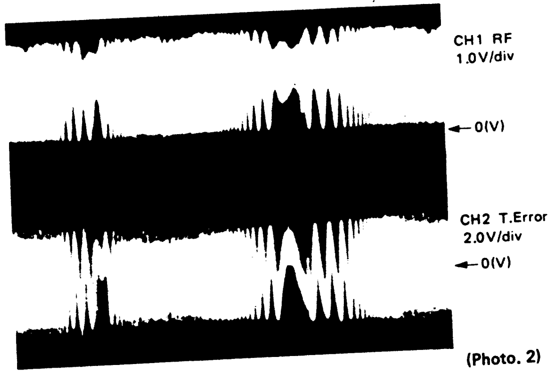
ADJUSTMENT/REGLAGE/ABGLEICH

4. Description of Signal Waveforms, Connection of Measuring Instruments/Description des formes d'onde des signaux, connexion des instruments de mesure/ Beschreibung der Signal-Wellenformen, Anschluß der Meßinstrumente



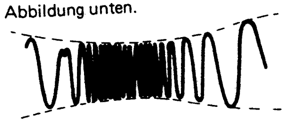
(Photo. 1)
(Photo. 1)
(Foto. 1)

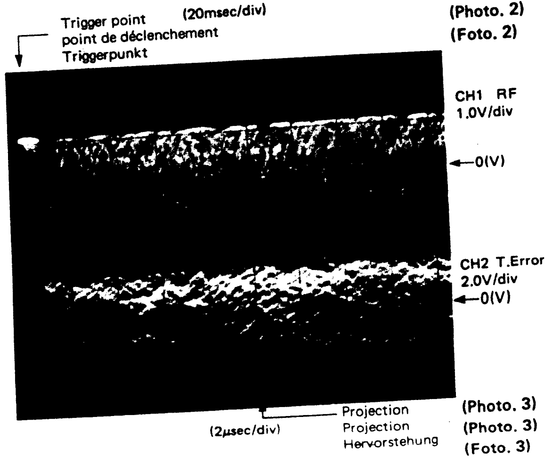
- RF signal and T.Error signal after diffraction grating adjustment.
- Signal RF et signal T.Error après ajustement de réseau de diffraction.
- RF-Signal und T.Error-Signal nach Diffraktions-gitter-Einstellung.



(Photo. 2)
(Photo. 2)
(Foto. 2)

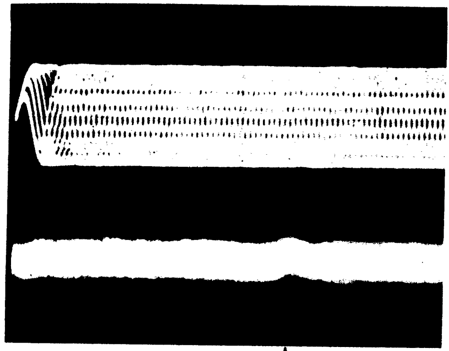
- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.
- Signal RF et signal T.Error quand il y a une petite erreur de position du réseau de diffraction.
- Le niveau de signal T.Error est petit et l'envelope est telle qu'indiquée dans le diagramme ci-dessous.
- RF-Signal und T.Error-Signal bei kleinem Diffraktionsgitter-Positionierungsfehler.
- Der T.Error-Signalpegel ist klein, und die Hüll-kurve ist wie in der Abbildung unten.





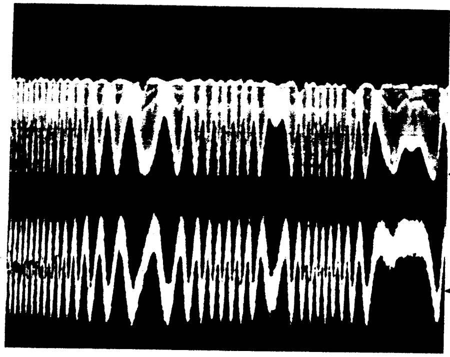
(Photo. 3)
(Photo. 3)
(Foto. 3)

- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observies in the T.Error waveform.
- Le signal RF et le signal T.Error en mode de test (avec la mise au point sur ON).
- Quand un faisceau auxiliaire tracela même série de bits que le faisceau principal pendant l'ajustement de réseau de diffraction, l'apport du point de déclenchement RF à la position indiquée dans la photo provoque une "projection" qui s'observe dans la forme d'onde d' T.Error.
- RF-Signal und T.Error-Signal im Testmodus (bei geschalteter Fokussierung).
- Wenn der Nebenstrahl die gleiche Bi
  Hauptstrahl während der Diffrak
  verfolgt und den RF-Trigg
  gezeigte Position brin
  verursacht, die in
  werden kann.



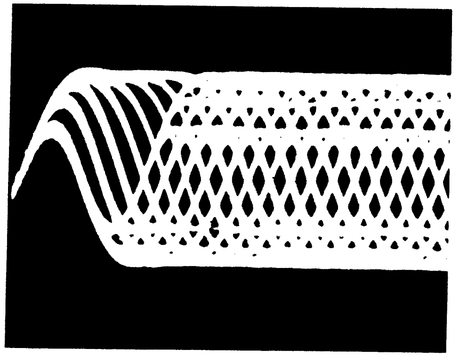
(Photo. 4)
(Photo. 4)
(Foto. 4)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 12μs after RF signal, in the form of a projection.
- Signal RF et signal E.Spot en mode de test (PLAY).
- Si le réseau de diffraction a été ajusté correctement, l'influence du déclenchement s'observe sur la forme d'onde E.Spot d'environ 12μs après le signal RF, sous la forme d'une projection.
- RF-Signal und E.Spot-Signal im Testmodus (PLAY).
- Wenn das Diffraktionsgitter richtig eingestellt wurde, wird der Einfluß des Triggers in der E.Spot-Wellenform etwa 12μs nach dem RF-Signal in der Form einer Hervorstehung beobachtet.



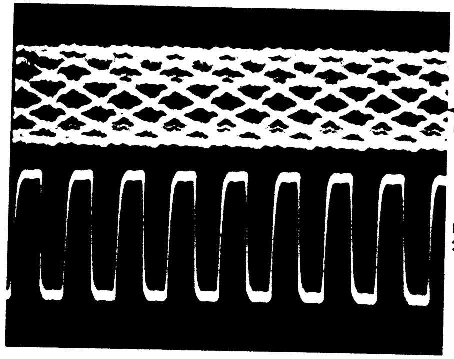
(Photo. 5)
(Photo. 5)
(Foto. 5)

- RF signal and T.Error signal; in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR3 of X29-1780-00)
- Signal RF et signal T.Error; en mode test (mise au point ON). (Disque de type 4)
- Ajuster T.Error pour que la forme d'onde soit symétrique en-dessus et au-dessous de 0V. (VR3 de X29-1780-00)
- RF-Signal und T.Error-Signal; im Testmodus (Fokussierung eingeschaltet). (Disc-Typ 4)
- T.Error so einstellen, daß die Wellenform über und unter 0V symmetrisch ist. (VR3 von X29-1780-00)



(Photo. 6)
(Photo. 6)
(Foto. 6)

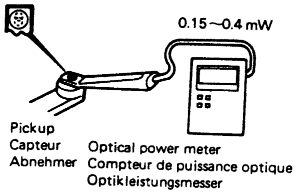
- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.
- Signal RF en mode de test (PLAY).
- Effectuer les ajustements d'offset tangentiel et de mise au point pour que chacun des points de croisement central soit mis au point sur un point de l'affichage. Les points de croisement au-dessus et en-dessous du centre doivent aussi être affichés clairement.
- RF-Signal im Testmodus (PLAY).
- Die Tangential- und Fokusversatz-Einstellungen so durchführen, daß jeder der mittleren Kreuzungspunkte in einem Punkt auf dem Display fokussiert wird. Auch die Kreuzungspunkte über und unter der Mitte müssen klar angezeigt werden.



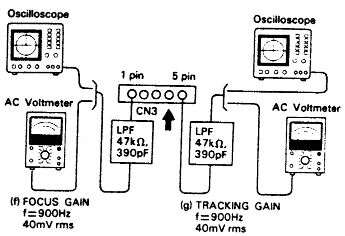
(Photo. 7)
(Photo. 7)
(Foto. 7)

- RF signal and PLCK signal in test mode (PLAY).
- When the synch system is normal, the cross points the center of the eye pattern shall coincide with PLCK fall points.
- Le signal RF et le signal PLCK en mode de test (PLA
- Quand le système sync est normal, les points de cro ment au centre de la forme oculaire doivent coïnci avec les points de chute PLCK.
- RF-Signal und PLCK-Signal im Testmodus (PLAY).
- Wenn das Sync-System normal ist, müssen die Kr zungspunkte in der Mitte des Augenmusters mit d PLCK-Fallpunkten zusammenfallen.

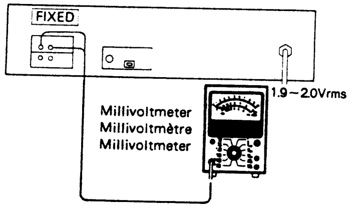
(a)


0.15~0.4 mW
Pickup
Capteur
Abnehmer
Optical power meter
Compteur de puissance optique
Optikleistungsmesser

(g)


Oscilloscope
Oscilloscope
1 pin
5 pin
CN3
AC Voltmeter
AC Voltmeter
LPF
47kΩ.
390pF
LPF
47kΩ.
390pF
(f) FOCUS GAIN
f=900Hz
40mV rms
(g) TRACKING GAIN
f=900Hz
40mV rms

(h)


FIXED
1.9~2.0Vrms
Millivoltmeter
Millivoltmètre
Millivoltmeter

DP-990SG

VOLTAGE CHECK TABLE

(X29-1870-00)

IC1

1	0V	16	1.3V
2	0V	17	−4.9V
3	0V	18	0V
4	4.5V	19	−0.1V
5	–	20	0V
6	−4.4V	21	−4.8V
7	0V	22	0V
8	0V	23	−3.4V
9	0V	24	0V
10	0V	25	0V
11	0V	26	2.4V
12	0V	27	2.7V
13	0V	28	0.1V
14	0V	29	–
15	−1.0V	30	4.9V

IC2

1	4.9V	8	0V
2	4.9V	9	2.7V
3	0V	10	2.7V
4	0V	11	4.9V
5	0V	12	2.7V
6	4.9V	13	0.1V
7	0V	14	4.9V

Q1

E	0.7V
B	0V
C	0V

(X25-3050-01)

IC1

1	−5.6V	9	0V
2	0V	10	−3.2V
3	4.9V	11	−3.2V
4	−4.8V	12	−3.2V
5	1.3V	13	−3.2V
6	2.4V	14	−3.2V
7	−0.1V	15	1.8V
8	−4.8V	16	5.7V

IC2

1	−5.6V	9	0V
2	0V	10	−3.2V
3	4.9V	11	−3.2V
4	−4.8V	12	−3.2V
5	1.3V	13	−3.2V
6	2.4V	14	−3.2V
7	−0.1V	15	1.8V
8	−4.8V	16	5.7V

1	0V
2	0V
3	0V
4	−15.6V
5	0V
6	0V
7	0V
8	15.5V

IC4

1	0V
2	0V
3	0V
4	−15.6V
5	0V
6	0V
7	0V
8	15.5V

IC5

1	0V
2	−0.1V
3	0V
4	−15.6V
5	0V
6	−0.1V
7	0V
8	15.V5

IC6

1	0V
2	0.1V
3	0V
4	−15.6V
5	0V
6	−0.1V
7	0V
8	15.5V

IC7

1	0V
2	−0.1V
3	0V
4	−15.6V
5	0V
6	−0.1V
7	0V
8	15.5V

IC8

1	0V
2	−0.1V
3	0V
4	−15.6V
5	0V
6	−0.1V
7	0V
8	15.5V

IC9

1	0V
2	0V
3	0V
4	−15.6V
5	0V
6	0V
7	0V
8	15.5V

IC10

1	0V
2	0V
3	0V
4	−15.6V
5	0V
6	0V
7	0V
8	15.5V

IC13

1	3.1V
2	0V
3	0V
4	−19.3V
5	5.1V
6	5.1V
7	−3.5V
8	19V

IC14

1	0V	21	0V	41	0V
2	4.7V	22	0V	42	0V
3	4.7V	23	0V	43	0V
4	2.2V	24	0V	44	4.9V
5	0V	25	1.2V	45	4.9V
6	2.4V	26	1.2V	46	4.9V
7	4.9V	27	0V	47	4.9V
8	0V	28	0V	48	4.9V
9	4.7V	29	4.2V	49	0V
10	4.9V	30	1.5V	50	4.7V
11	4.9V	31	0V	51	4.7V
12	0V	32	2.4V	52	4.7V
13	2.0V	33	2.4V	53	4.7V
14	2.6V	34	2.4V	54	0V
15	0V	35	0V	55	4.7V
16	4.9V	36	0.1V	56	4.7V
17	4.7V	37	0.1V	57	4.7V
18	0V	38	0V	58	4.7V
19	0V	39	0V	59	4.7V
20	4.9V	40	0V	60	4.9V

IC15

1	−0.1V	23	4.9V
2	0V	24	0V
3	0V	25	0V
4	0V	26	0V
5	1.3V	27	0V
6	0V	28	0V
7	2.4V	29	0V
8	0V	30	0V
9	0V	31	0V
10	0V	32	0V
11	−0.1V	33	0V
12	2.1V	34	4.9V
13	1.2V	35	0V
14	1.5V	36	4.9V
15	2.3V	37	0V
16	0V	38	0V
17	4.9V	39	4.9V
18	4.9V	40	2.4V
19	4.9V	41	1.8V
20	0V	42	0V
21	4.9V	43	0V
22	0V	44	2V

IC16

IN	−15.6V
OUT	−5.9V
GND	0V

IC17

IN	15.5V
OUT	5.9V
GND	0V

IC22

IN	−19.6V
OUT	−5.1V
GND	0V

IC23

IN	19.3V
OUT	5V
GND	0V

IC24

IN	4.9V
OUT	4.9V
GND	0V

Q2

E	15.5V
B	16.1V
C	19.1V

Q3

E	−15.6V
B	−16.2V
C	−19.4V

Q10

E	0V
B	0.2V
C	15.5V

Q11

E	0V
B	0.2V
C	15.5V

Q12

E	0V
B	0V
C	1.1V

Q13

E	0V
B	0V
C	1.1V

Q14

E	15.5V
B	14.7V
C	15.5V

(X32-1170-01)

IC1

1	0V	16	0.1V
2	0V	17	−4.9V
3	0V	18	−4.4V
4	0V	19	0V
5	0V	20	0V
6	0V	21	−0.1V
7	4.9V	22	0V
8	4.9V	23	0.6V
9	4.9V	24	0V
10	4.9V	25	0V
11	0V	26	4.9V
12	0V	27	−0.7V
13	0V	28	0V
14	−4.2V	29	0V
15	4.9V	30	0V

IC2

1	0V	9	0V
2	0V	10	0V
3	0V	11	0V
4	0V	12	−0.1V
5	0V	13	0V
6	0V	14	−0.1V
7	−4.9V	15	0V
8	0V	16	4.9V

IC3

1	−0.6V	5	0V
2	0V	6	0V
3	0V	7	0V
4	−4.9V	8	4.9V

IC4

1	0.5V	5	0V
2	0V	6	0V
3	0V	7	0.5V
4	−10.3V	8	10.0V

IC5

1	0V	5	0V
2	2.4V	6	0V
3	2.4V	7	0.6V
4	−10.3V	8	10V

IC7

1	2.3V	13	0.6V
2	2.3V	14	0.6V
3	2.3V	15	2.6V
4	2.3V	16	2.1V
5	2.3V	17	4.2V
6	2.0V	18	2.0V
7	2.3V	19	2.3V
8	2.6V	20	2.0V
9	2.6V	21	4.2V
10	2.6V	22	2.3V
11	0.6V	23	2.3V
12	0V	24	4.9V

(X32-1170-01)

IC6

1	0V	41	2.4V
2	0V	42	2.4V
3	0V	43	2.4V
4	0V	44	2.4V
5	0V	45	2.4V
6	0V	46	2.2V
7	0V	47	0V
8	2.4V	48	0V
9	2.4V	49	0V
10	0V	50	0V
11	2.4V	51	0V
12	0V	52	0V
13	4.9V	53	1.4V
14	4.9V	54	2.3V
15	4.9V	55	0V
16	4.9V	56	0V
17	0V	57	4.9V
18	4.9V	58	0V
19	4.9V	59	0V
20	0V	60	1.2V
21	4.9V	61	1.2V
22	0V	62	3.6V
23	0V	63	3.6V
24	0V	64	1.9V
25	2.4V	65	1.9V
26	0V	66	1.9V
27	2.1V	67	4.9V
28	0V	68	2.4V
29	0.6V	69	2.4V
30	0.6V	70	1.6V
31	0.6V	71	4.9V
32	2.7V	72	4.9V
33	4.9V	73	4.9V
34	2.7V	74	2.4V
35	2.7V	75	2.4V
36	2.2V	76	2.4V
37	4.2V	77	–
38	2.4V	78	0V
39	2.4V	79	2.4V
40	2.4V	80	2.4V

IC9

1	0V	8	0V
2	4.9V	9	4.9V
3	0V	10	0V
4	4.9V	11	0V
5	0V	12	–
6	0V	13	2.1V
7	0V	14	4.9V

IC11

RST	4.8V
GND	0V
5	4.9V

IC12

1	5.6V
2	5.1V
3	5.1V
4	5.1V
5	0V
6	5.1V
7	0V
8	0V
9	4.9V

IC10

1	2.9V	33	0V
2	3.5V	34	0V
3	3.5V	35	0V
4	3.2V	36	0V
5	3.2V	37	0V
6	0V	38	0V
7	2.4V	39	4.8V
8	0V	40	0.3V
9	0V	41	0.3V
10	4.8V	42	0.3V
11	0V	43	0.3V
12	0V	44	0.3V
13	0V	45	0.3V
14	0V	46	0.3V
15	4.9V	47	0.3V
16	4.9V	48	0.3V
17	4.9V	49	0.3V
18	0.6V	50	0.3V
19	4.9V	51	0.3V
20	0.6V	52	0.3V
21	0V	53	0.3V
22	0V	54	1.3V
23	0V	55	1.3V
24	0V	56	0V
25	4.9V	57	0V
26	4.9V	58	0.9V
27	0V	59	3.1V
28	0V	60	0.3V
29	0V	61	0.6V
30	1.6V	62	2.2V
31	0V	63	1.6V
32	0V	64	4.9V

IC13

1	5.1V	9	−39V
2	5.1V	10	–
3	5.1V	11	0V
4	5.1V	12	−8.2V
5	3.2V	13	5.3V
6	3.5V	14	5.3V
7	0V	15	5.3V
8	6.6V	16	5.3V

IC14

1	2.9V	9	−39V
2	2.2V	10	0V
3	0.3V	11	−35.7V
4	0.9V	12	−26.7V
5	1.3V	13	−29.2V
6	0.3V	14	−38.3V
7	0V	15	−16.9V
8	6.6V	16	10.9V

IC15

1	3.5V	9	−39V
2	1.6V	10	0V
3	0.6V	11	−36V
4	3.1V	12	−26V
5	1.3V	13	−8.2V
6	0.3V	14	−31.7V
7	0V	15	−22.8V
8	6.6V	16	−5.4V

IC16

1	0.3V	9	−39V
2	0.3V	10	0V
3	0.3V	11	−36V
4	0.3V	12	−36V
5	0.3V	13	−36V
6	0.3V	14	−36V
7	0V	15	−36V
8	6.6V	16	−36V

IC17

1	0.3V	9	−39V
2	0.3V	10	0V
3	0.3V	11	−36V
4	0.3V	12	−36V
5	0.3V	13	−36V
6	0.3V	14	−36V
7	0V	15	−36V
8	6.6V	16	−36V

IC18

1	10V
2	0V
3	4.9V

IC19

1	−0.6V
2	0V
3	0V
4	−15.6V
5	0V
6	0V
7	−0.6V
8	15.5V

IC20

1	−5.5V
2	0V
3	0V
4	−10.2V
5	0V
6	0V
7	0.6V
8	9.8V

(X32-1170-01)

Q1

E	0V
B	−4.9V
C	0V

Q2

E	0V
B	−0.6V
C	10V

Q3

E	0V
B	−0.6V
C	−10.3V

Q4

E	0V
B	−0.7V
C	10V

Q5

E	0V
B	−0.7V
C	−10.3V

Q6

E	0V
B	−0.5V
C	10V

Q7

E	0V
B	−0.5V
C	−10.3V

Q8

E	0V
B	0.5V
C	10.0V

Q9

E	0V
B	0.5V
C	−10.3V

Q10

E	0V
B	0.6V
C	10V

Q11

E	0V
B	0.6V
C	−10.3V

Q12

E	0V
B	0.5V
C	10V

Q13

E	0V
B	0.5V
C	−10.3V

Q14

E	6.6V
B	7.3V
C	10.0V

Q15

E	0V
B	0.6V
C	0V

Q16

E	4.9V
B	4.3V
C	4.9V

Q17

E	7.5V
B	8.1V
C	15.4V

Q18

E	−32.5V
B	−33.1V
C	−39V

Q19

E	−4.9V
B	–
C	−10.3V

Q20

E	0V
B	0.5V
C	10V

Q21

E	0.1V
B	0.6V
C	19.1V

Q22

E	0.1V
B	0.6V
C	19.1V

Q23

E	0.1V
B	−0.6V
C	−19V

Q24

E	0.1V
B	−0.6V
C	−19V

Q25

E	4.9V
B	0V
C	4.8V

Q26

E	4.9V
B	4.9V
C	−4.9V

(X25-3040-1)

IC1

1	0V
2	4.9V
3	4.9V

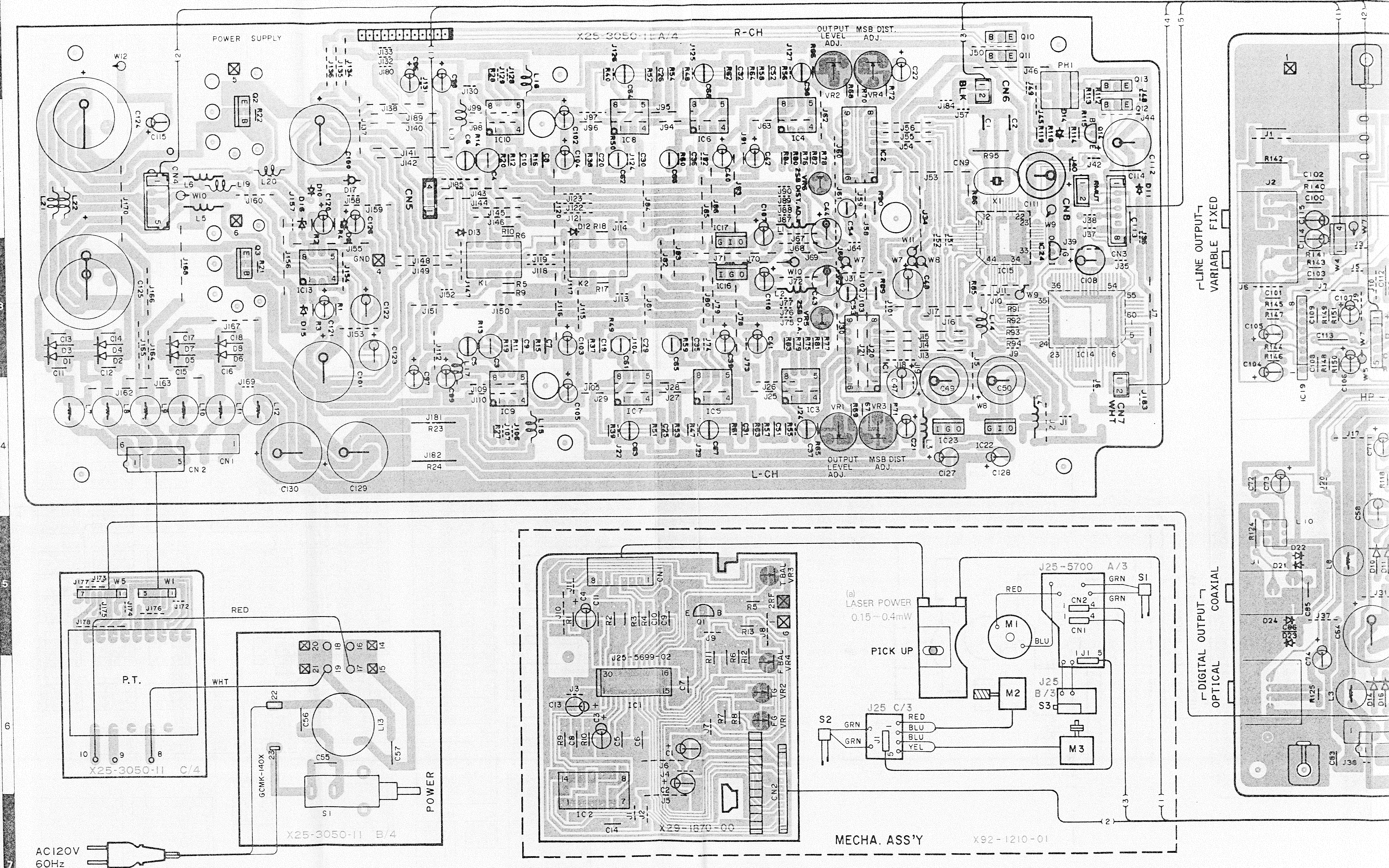
IC2

1	4.9V	9	0.3V
2	0V	10	0V
3	1.0V	11	1.9V
4	1.0V	12	0V
5	0V	13	1.6V
6	2.9V	14	0.3V
7	4.8V	15	0V
8	0V	16	4.9V

IC3

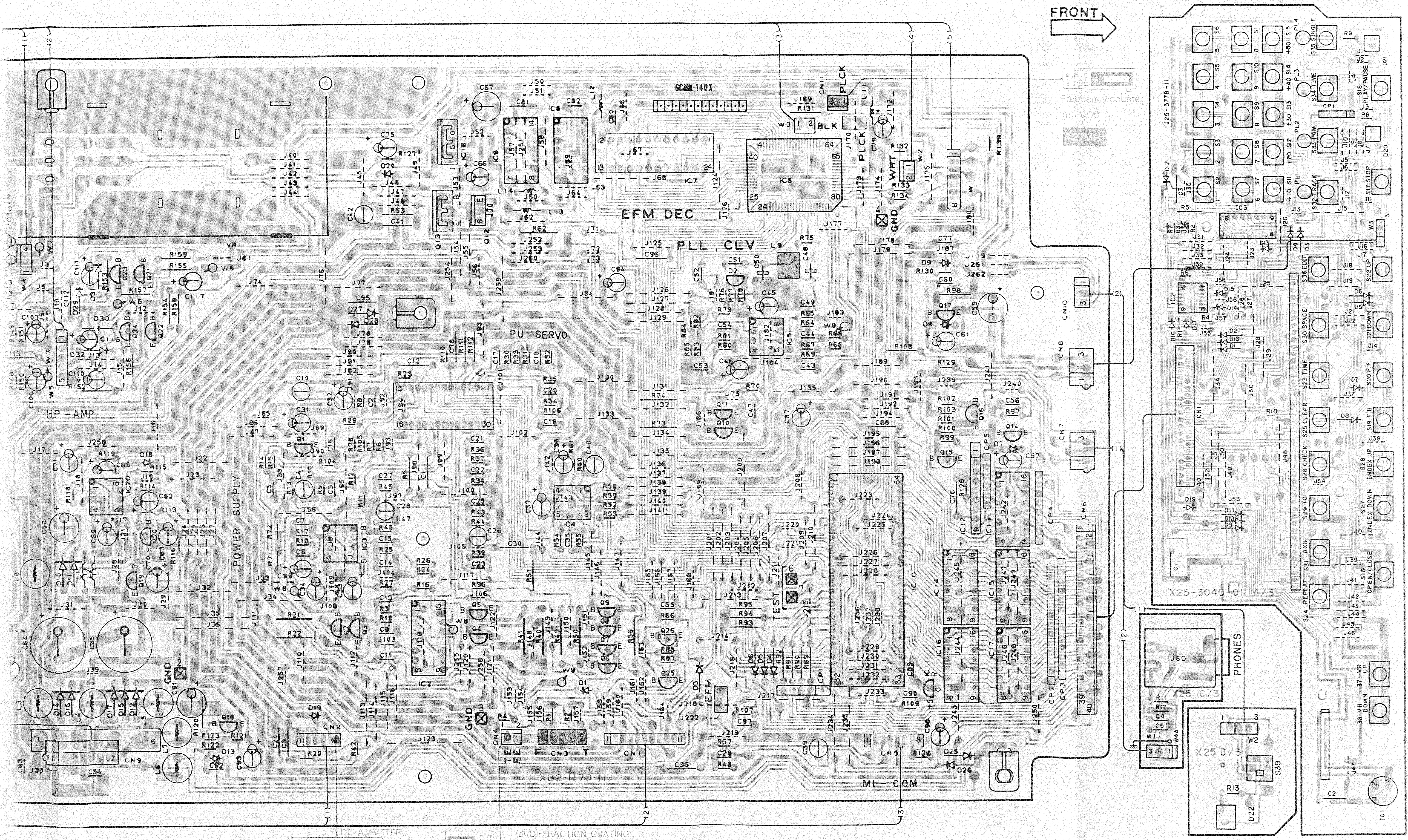
1	4.8V	9	7.5V
2	0V	10	0V
3	0V	11	0V
4	0V	12	0V
5	0V	13	7.5V
6	0V	14	7.5V
7	0V	15	7.5V
8	0V	16	0.8V

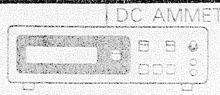
PC BOARD (COMPONENT SIDE VIEW)

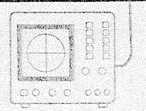


POWER SUPPLY
X25-3050-11 A/4
R-CH
OUTPUT LEVEL ADJ.
MSB DIST. ADJ.
VR2
VR4
VR1
VR3
L-CH
CN1
CN2
CN4
CN5
CN6
BLK
CN7
WHT
CN8
CN9
CN3
PH1
GND
K1
K2
X1
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC13
IC14
IC15
IC16
IC17
IC22
IC23
C129
C130
C124
C125
C127
C128
Q10
Q11
Q12
Q13
┌LINE OUTPUT┐
VARIABLE FIXED
┌DIGITAL OUTPUT┐
OPTICAL COAXIAL
HP
P.T.
RED
WHT
W1
W5
X25-3050-11 C/4
C55
C56
C57
L13
GCMK-140X
S1
POWER
X25-3050-11 B/4
AC120V
60Hz
J25-5699-02
X29-1670-00
(a) LASER POWER
0.15～0.4mW
PICK UP
M1
M2
M3
BLU
RED
GRN
J25-5700 A/3
J25 B/3
J25 C/3
S1
S2
S3
RED
BLU
BLU
YEL
MECHA. ASS'Y
X92-1210-01

Refer to the schematic diagram for the values of resistors and capacitors.


FRONT
Frequency counter
(c) VCO
4.27MHz
EFM DEC
PLL . CLV
PU SERVO
POWER SUPPLY
HP-AMP
MI-COM
GCAMN-140X
X32-1170-11
X25-5778-11
X25-3040-01 A/3
X25 C/3
X25 B/3
PHONES
TEST
GND
IEFM
PLCK
BLK
WHT
S35 SINGLE
S34 TIME
S33 PGM
S32 TRACK
S17 STOP
S18 PLAY/PAUSE
S36 EDIT
S22 UP
S30 SPACE
S21 DOWN
S23 TIME
S20 F.F
S25 CLEAR
S19 F.B
S26 CHECK
S28 INDEX UP
S29 TO
S27 INDEX DOWN
S31 AXB
S16 OPEN/CLOSE
S24 REPEAT
37 VR UP
36 VR DOWN





(b) LASER PICKUP:
+5.5 mA current value labeled on the laser pickup

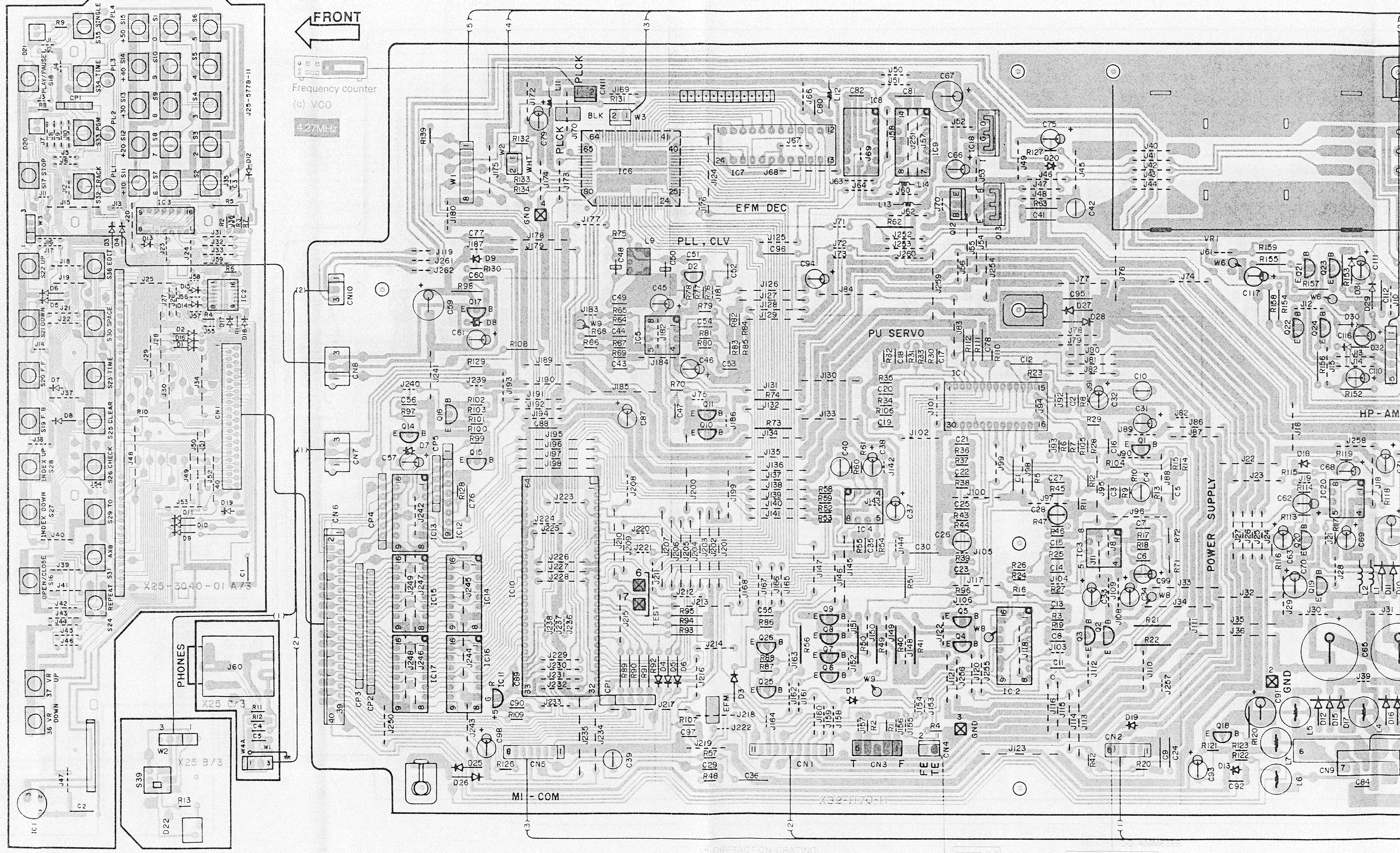
(d) DIFFRACTION GRATING:
Check that the diffraction grating is aligned correctly.

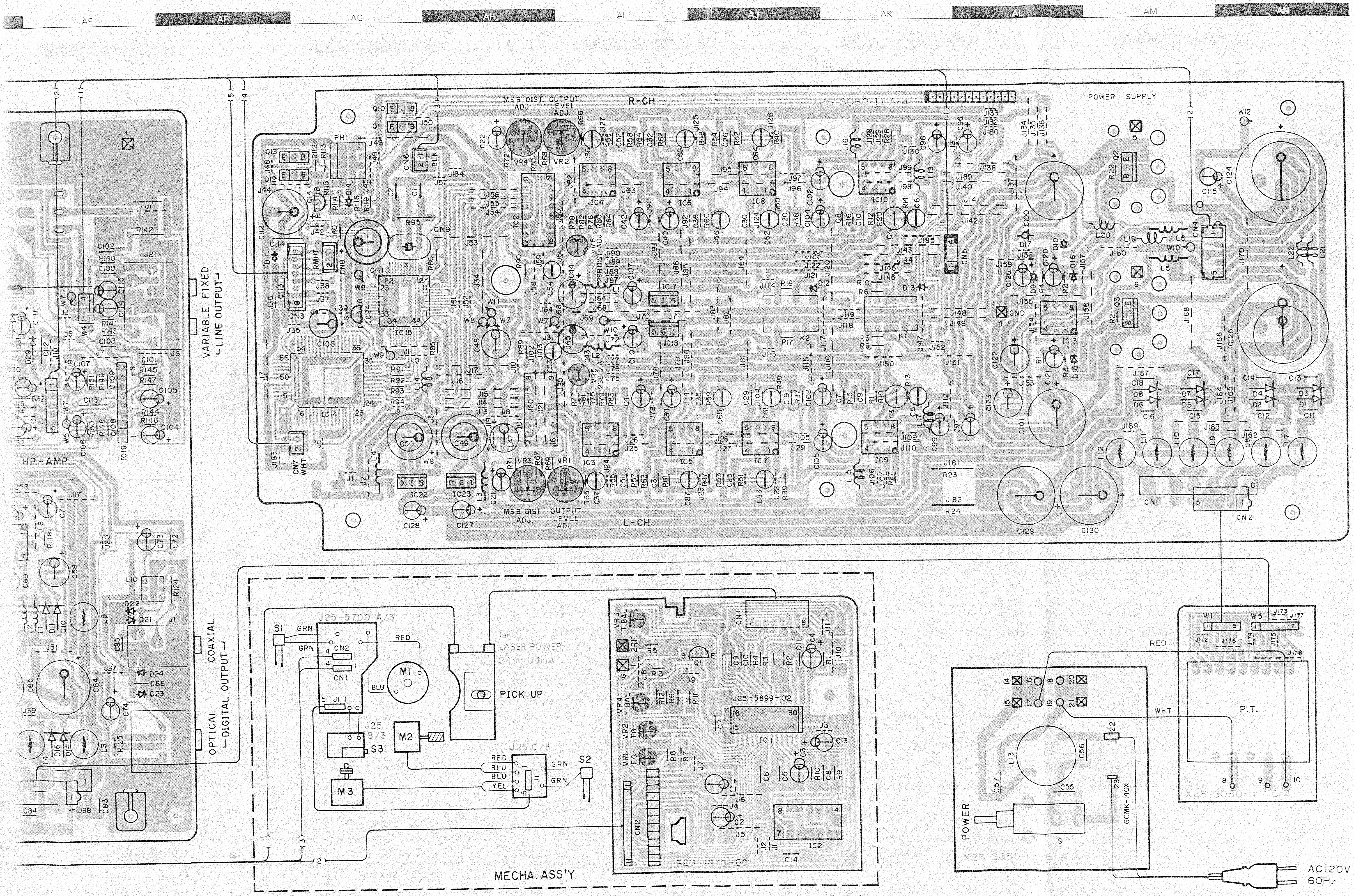
(e) TRACKING ERROR BALANCE:
Symmetry between upper and lower patterns, or DC=0±0.05 V

(f) FOCUS ERROR BALANCE: Optimum eye pattern

DP-990SG(K)

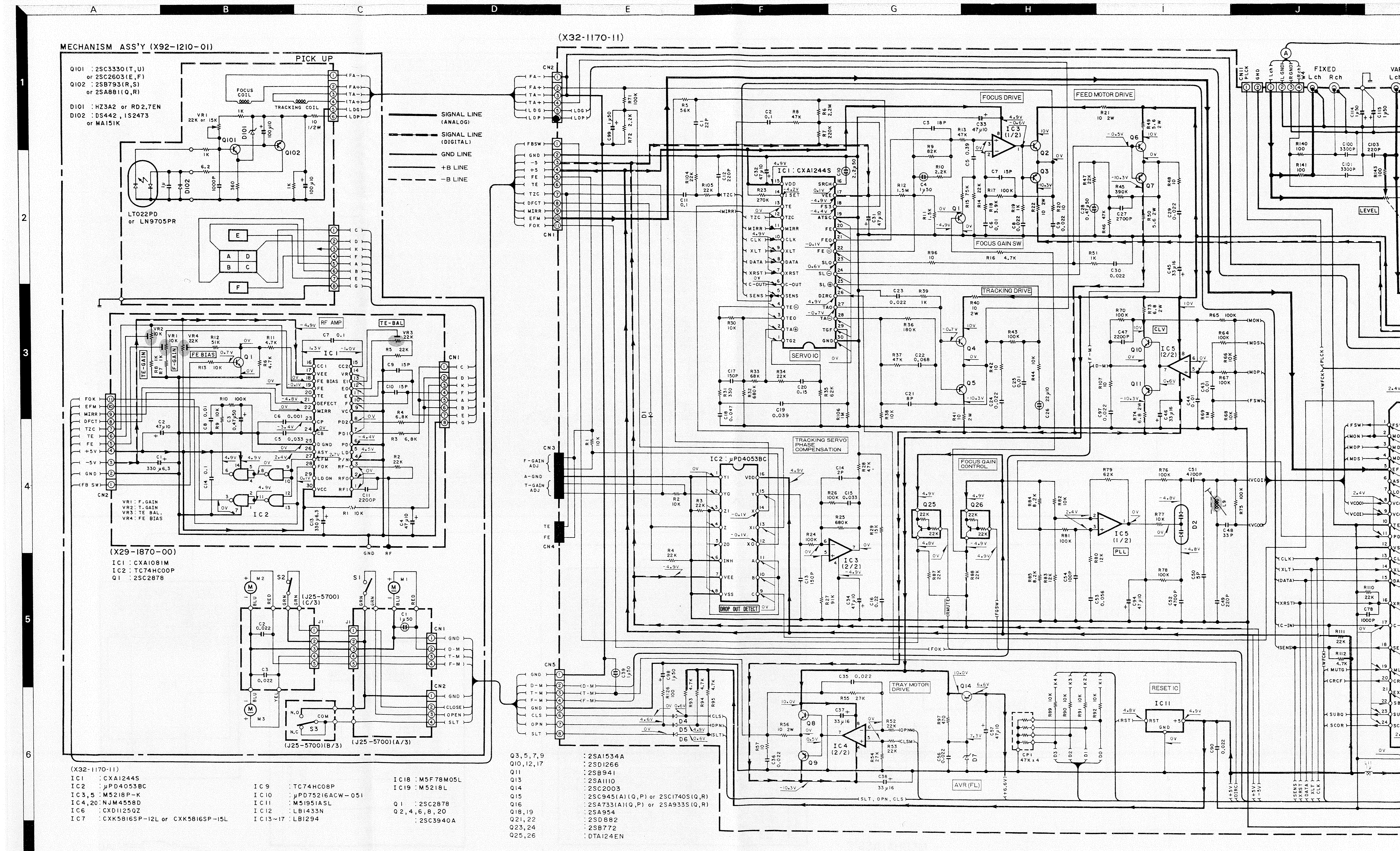
PC BOARD (FOIL SIDE VIEW)


FRONT
Frequency counter
(c) VCO
4.27MHz
PHONES
X25-3040-01 A/3
X25 C/3
X25 B/3
J25-5778-11
EFM DEC
PLL, CLV
PU SERVO
MI-COM
POWER SUPPLY
HP-AM
TEST
GND
EFM
FE
TE
X32-1170-11
(d) DIFFRACTION GRATING
Check that the diffraction grating is aligned correctly.
(e) TRACKING ERROR BALANCE


AE
AF
AG
AH
AI
AJ
AK
AL
AM
AN
X25-3050-11 A/4
MSB DIST. ADJ.
OUTPUT LEVEL ADJ.
R-CH
L-CH
POWER SUPPLY
VARIABLE FIXED
—LINE OUTPUT—
HP-AMP
OPTICAL COAXIAL
—DIGITAL OUTPUT—
J25-5700 A/3
J25 B/3
J25 C/3
(a) LASER POWER: 0.15～0.4mW
PICK UP
M1
M2
M3
S1
S2
S3
RED
BLU
GRN
YEL
WHT
J25-5699-02
X29-1870-00
X92-1210-01
MECHA. ASS'Y
P.T.
X25-3050-11 C/4
X25-3050-11 B/4
POWER
GCMK-140X
AC120V 60Hz
2SB DIST. ADJ.
2SB D.A.
GND
CN1
CN2
BLK

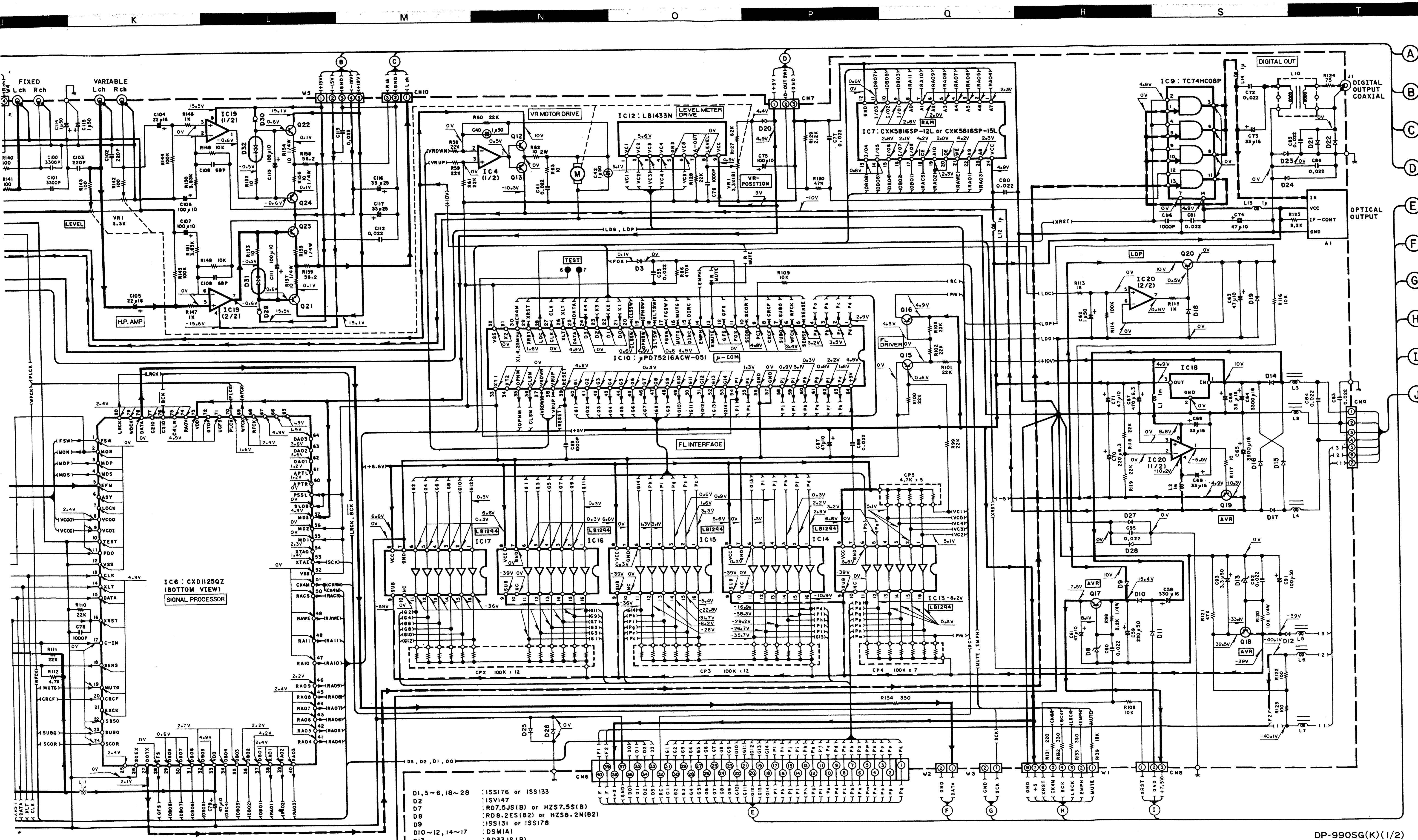
Refer to the schematic diagram for the values of resistors and capacitors.

DP-990SG(K)


A
B
C
D
E
F
G
H
I
J
1
2
3
4
5
6
7
MECHANISM ASS'Y (X92-1210-01)
PICK UP
Q101 : 2SC3330(T,U) or 2SC2603(E,F)
Q102 : 2SB793(R,S) or 2SA881(Q,R)
D101 : HZ3A2 or RD2.7EN
D102 : DS442, 1S2473 or MA151K
FOCUS COIL
TRACKING COIL
VR1 22K or 15K
LT022PD or LN9705PR
FA−
FA+
TA−
TA+
LDG
LDP
SIGNAL LINE (ANALOG)
SIGNAL LINE (DIGITAL)
GND LINE
+B LINE
−B LINE
(X32-1170-11)
CN1
CN2
CN3
CN4
CN5
CN11
FBSW
GND
−5
+5
FE
TE
TZC
DFCT
MIRR
EFM
FOK
F-GAIN ADJ
A-GND
T-GAIN ADJ
RF AMP
TE-BAL
TE-GAIN
F-GAIN
FE BIAS
IC1
IC2
VR1 : F.GAIN
VR2 : T.GAIN
VR3 : TE BAL.
VR4 : FE BIAS
(X29-1870-00)
IC1 : CXA1081M
IC2 : TC74HC00P
Q1 : 2SC2878
GND
RF
M1
M2
M3
S1
S2
S3
BLU
RED
GRN
YEL
J1
(J25-5700) (C/3)
(J25-5700)(B/3)
(J25-5700)(A/3)
N.O
N.C
COM
D-M
T-M
F-M
CLOSE
OPEN
SLT
CLS
OPN
IC1 : CXA1244S
SERVO IC
FOCUS DRIVE
FEED MOTOR DRIVE
FOCUS GAIN SW
TRACKING DRIVE
CLV
IC3 (1/2)
IC3 (2/2)
IC5 (1/2)
IC5 (2/2)
PLL
IC2 : µPD4053BC
DROP OUT DETECT
TRACKING SERVO PHASE COMPENSATION
FOCUS GAIN CONTROL
TRAY MOTOR DRIVE
IC4 (2/2)
AVR (FL)
RESET IC
IC11
CP1 47K×4
FIXED
VAR
Lch
Rch
LEVEL
PLCK
GND
(WFCK)
(PLCK)
MON
MDS
MDP
FSW
VCOI
VCOO
CLK
XLT
DATA
XRST
C-IN
SENS
MUTG
CRCF
SUBQ
SCOR
RST
SLT, OPN, CLS
(MUTE)
(FGSW)
(FOK)
(+6.6V)

(X32-1170-11)

IC1	: CXA1244S
IC2	: µPD4053BC
IC3,5	: M5218P-K
IC4,20	: NJM4558D
IC6	: CXD1125QZ
IC7	: CXK5816SP-12L or CXK5816SP-15L
IC9	: TC74HC08P
IC10	: µPD75216ACW-051
IC11	: M51951ASL
IC12	: LB1433N
IC13~17	: LB1294
IC18	: M5F78M05L
IC19	: M5218L
Q1	: 2SC2878
Q2,4,6,8,20	: 2SC3940A
Q3,5,7,9	: 2SA1534A
Q10,12,17	: 2SD1266
Q11	: 2SB941
Q13	: 2SA1110
Q14	: 2SC2003
Q15	: 2SC945(A)(Q,P) or 2SC1740S(Q,R)
Q16	: 2SA733(A)(Q,P) or 2SA933S(Q,R)
Q18,19	: 2SA954
Q21,22	: 2SD882
Q23,24	: 2SB772
Q25,26	: DTA124EN



K
L
M
N
O
P
Q
R
S
T
FIXED
VARIABLE
Lch Rch
LEVEL
VR1 3.3K
H.P. AMP
IC19 (1/2)
IC19 (2/2)
VR MOTOR DRIVE
IC4 (1/2)
IC12 : LB1433N
LEVEL METER DRIVE
VR-POSITION
IC7 : CXK5816SP-12L or CXK5816SP-15L
RAM
IC9 : TC74HC08P
DIGITAL OUT
DIGITAL OUTPUT COAXIAL
OPTICAL OUTPUT
TEST
IC10 : μPD75216ACW-051
μ-COM
FL DRIVER
FL INTERFACE
LDP
IC20 (2/2)
IC18
IC20 (1/2)
AVR
IC6 : CXD1125QZ (BOTTOM VIEW)
SIGNAL PROCESSOR
IC17
IC16
IC15
IC14
IC13
LB1294
CP2 100K × 12
CP3 100K × 12
CP4 100K × 7
CP5 4.7K × 5
CN6
CN7
CN8
CN9
CN10
W1
W2
W3
W5
A
B
C
D
E
F
G
H
I
J

D1,3~6,18~28	:1SS176 or 1SS133
D2	:1SV147
D7	:RD7.5JS(B) or HZS7.5S(B)
D8	:RD8.2ES(B2) or HZS8.2N(B2)
D9	:1SS131 or 1SS178
D10~12,14~17	:DSM1A1
D13	:RD33JS(B)
D29,30	:E-272
D31,32	:MA27W

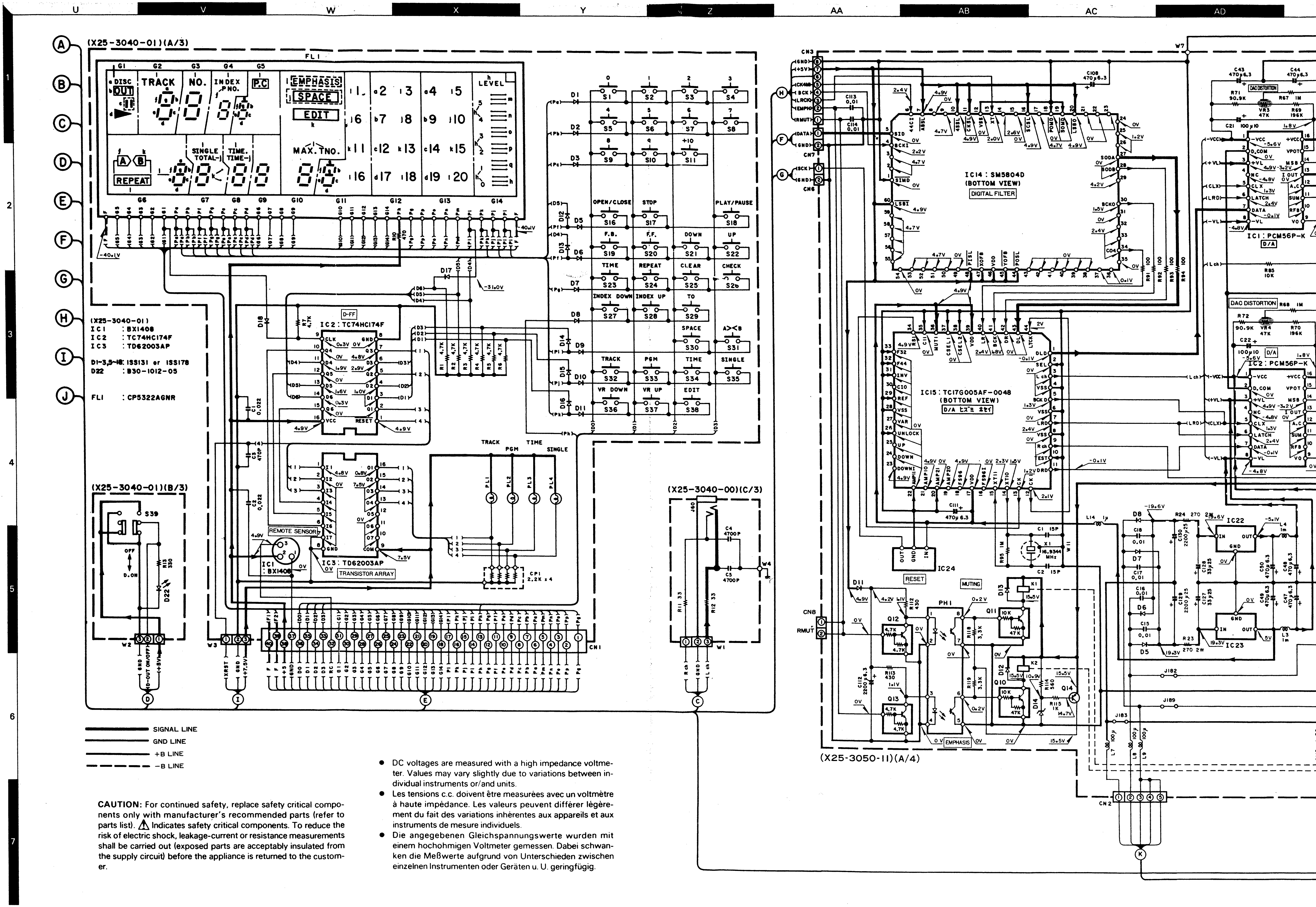
DP-990SG(K)(1/2)

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

DP-990SG

KENWOOD

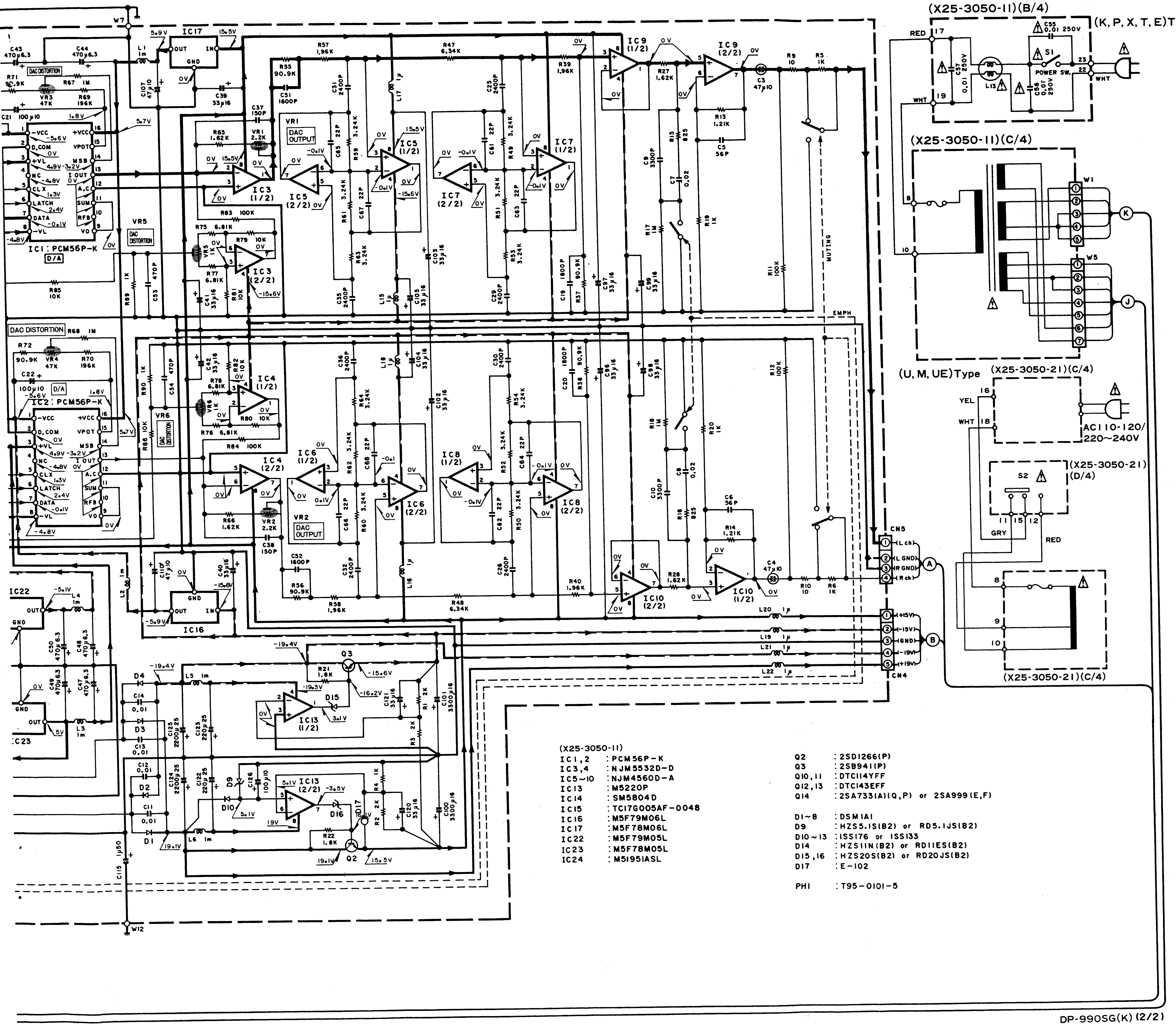


U
V
W
X
Y
Z
AA
AB
AC
AD
1
2
3
4
5
6
7
(X25-3040-01)(A/3)
FL1
DISC
OUT
TRACK
NO.
INDEX
P.NO.
P.C
EMPHASIS
SPACE
EDIT
MAX. TNO.
SINGLE
TOTAL-j
TIME.
TIME-j
REPEAT
LEVEL
(X25-3040-01)
IC1 : BX1408
IC2 : TC74HC174F
IC3 : TD62003AP
D1-3,5-16 : 1SS131 or 1SS178
D22 : B30-1012-05
FL1 : CP5322AGNR
IC2 : TC74HC174F
D-FF
IC3 : TD62003AP
TRANSISTOR ARRAY
REMOTE SENSOR
IC1 : BX1408
OPEN/CLOSE
STOP
PLAY/PAUSE
F.B.
F.F.
DOWN
UP
TIME
REPEAT
CLEAR
CHECK
INDEX DOWN
INDEX UP
TO
SPACE
A><B
TRACK
PGM
TIME
SINGLE
VR DOWN
VR UP
EDIT
PL1
PL2
PL3
PL4
CP1 2.2K x 4
(X25-3040-01)(B/3)
S39
OFF
D.ON
(X25-3040-00)(C/3)
CN1
W1
W2
W3
W4
W7
CN2
CN3
CN6
CN7
CN8
RMUT
IC14 : SM5804D
(BOTTOM VIEW)
DIGITAL FILTER
IC15 : TC17G005AF-0048
(BOTTOM VIEW)
D/A ヒズミ ホセイ
X1 16.9344 MHz
IC24
RESET
MUTING
PH1
EMPHASIS
IC1 : PCM56P-K
D/A
IC2 : PCM56P-K
DAC DISTORTION
IC22
IC23
(X25-3050-11)(A/4)

SIGNAL LINE
GND LINE
+B LINE
−B LINE

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhèrentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

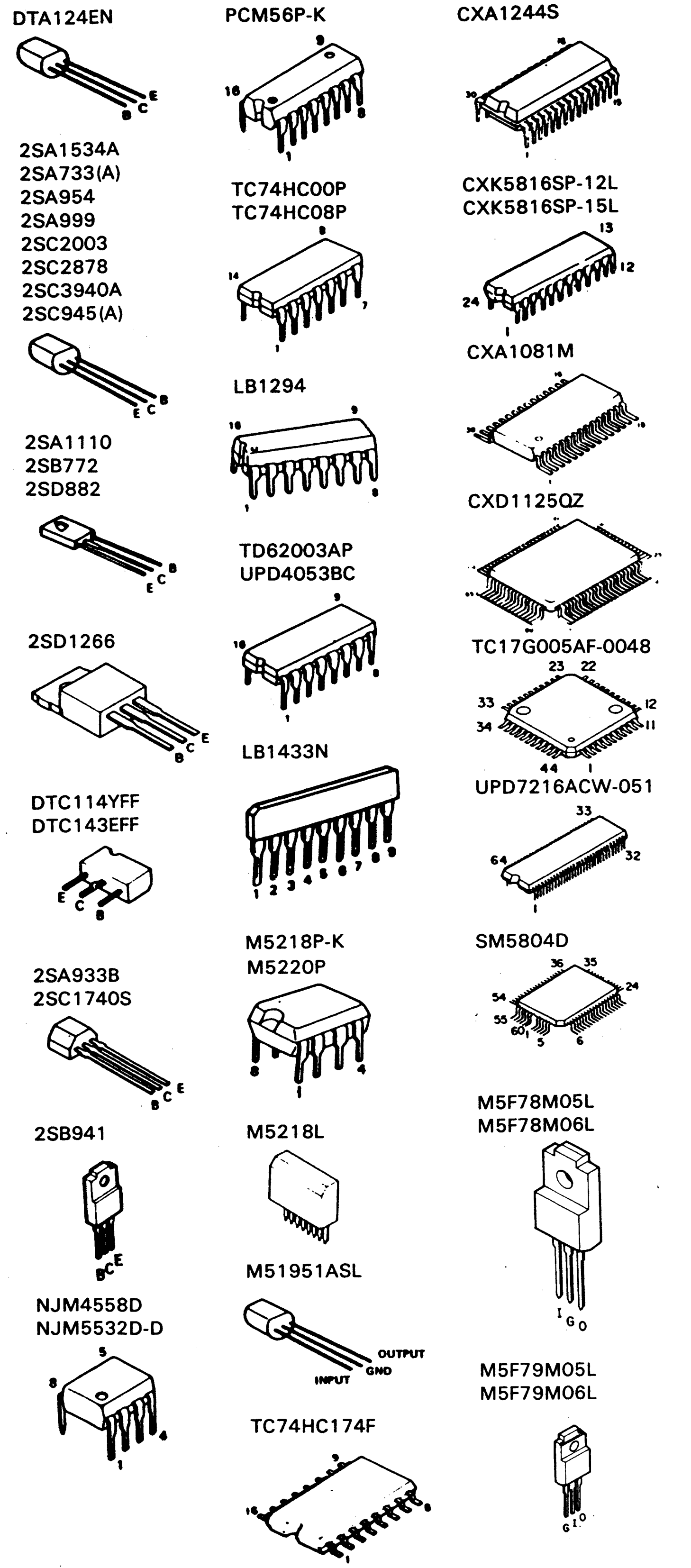

(X25-3050-11)(B/4)
(K, P, X, T, E)Type
RED
WHT
POWER SW.
S1
C55 0.01 250V
C57 0.01 250V
C56 0.01 250V
L13
(X25-3050-11)(C/4)
W1
W5
(U, M, UE)Type
(X25-3050-21)(C/4)
YEL
AC110-120/220~240V
(X25-3050-21)(D/4)
S2
GRY
(X25-3050-21)(C/4)
CN5
(L ch)
(L GND)
(R GND)
(R ch)
CN4
(+15V)
(-15V)
(GND)
(-19V)
(+19V)
EMPH
MUTING
IC1 : PCM56P-K
D/A
IC2 : PCM56P-K
IC3 (1/2)
IC3 (2/2)
IC4 (1/2)
IC4 (2/2)
IC5 (1/2)
IC5 (2/2)
IC6 (1/2)
IC6 (2/2)
IC7 (1/2)
IC7 (2/2)
IC8 (1/2)
IC8 (2/2)
IC9 (1/2)
IC9 (2/2)
IC10 (1/2)
IC10 (2/2)
IC13 (1/2)
IC13 (2/2)
IC16
IC17
IC22
IC23
DAC DISTORTION
VR1 DAC OUTPUT
VR2 DAC OUTPUT
VR3 47K
VR4 47K
VR5
VR6
Q2
Q3
D1
D2
D3
D4
D9
D10
D15
D16
D17
W7
W12
DP-990SG(K) (2/2)

(X25-3050-11)
IC1,2 : PCM56P-K
IC3,4 : NJM5532D-D
IC5~10 : NJM4560D-A
IC13 : M5220P
IC14 : SM5804D
IC15 : TC17G005AF-0048
IC16 : M5F79M06L
IC17 : M5F78M06L
IC22 : M5F79M05L
IC23 : M5F78M05L
IC24 : M51951ASL

Q2 : 2SD1266(P)
Q3 : 2SB941(P)
Q10,11 : DTC114YFF
Q12,13 : DTC143EFF
Q14 : 2SA733(A)(Q,P) or 2SA999(E,F)

D1~8 : DSM1A1
D9 : HZS5.1S(B2) or RD5.1JS(B2)
D10~13 : 1SS176 or 1SS133
D14 : HZS11N(B2) or RD11ES(B2)
D15,16 : HZS20S(B2) or RD20JS(B2)
D17 : E-102

PH1 : T95-0101-5

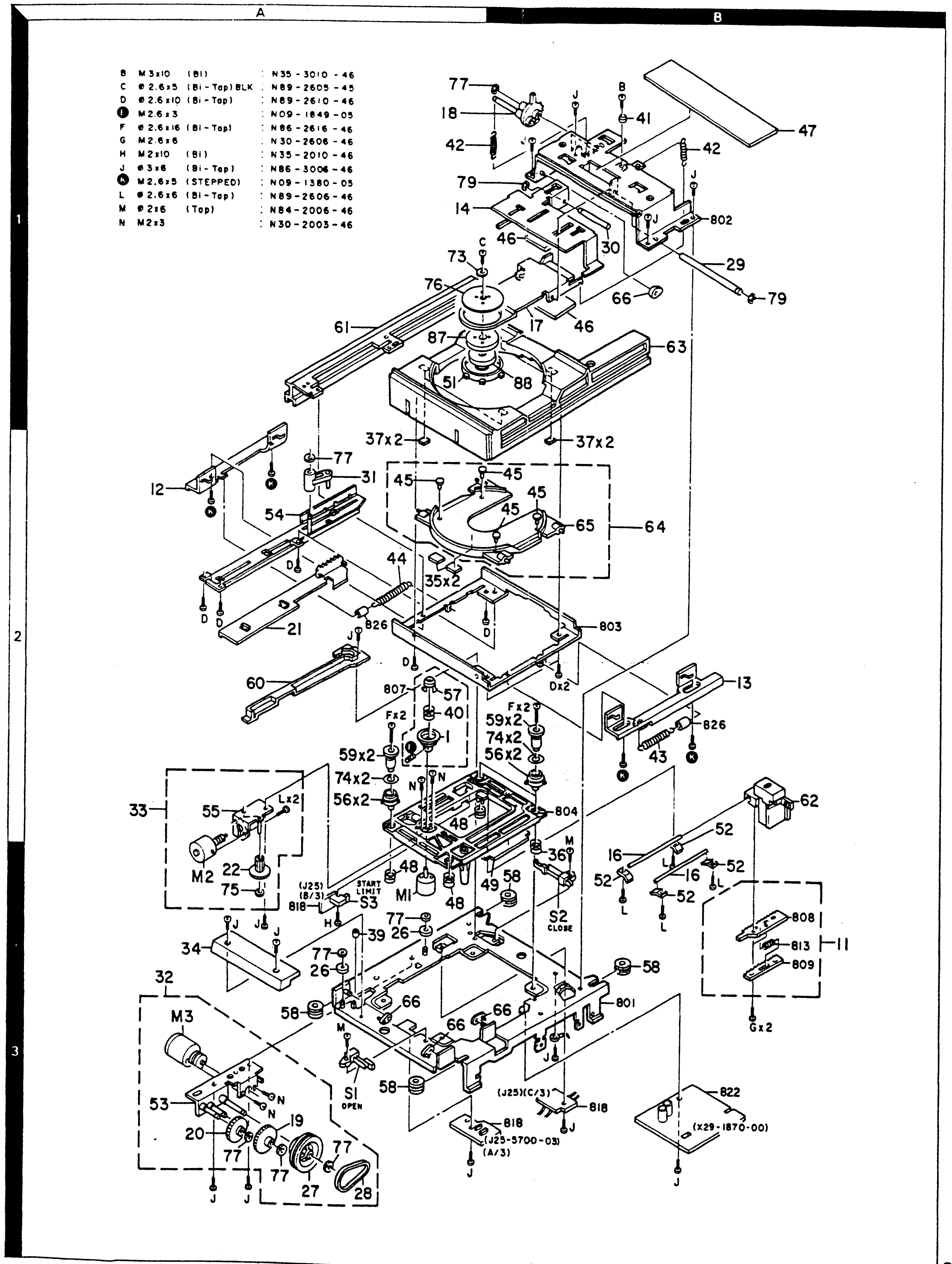

DTA124EN
E
C
B
2SA1534A
2SA733(A)
2SA954
2SA999
2SC2003
2SC2878
2SC3940A
2SC945(A)
2SA1110
2SB772
2SD882
2SD1266
DTC114YFF
DTC143EFF
2SA933B
2SC1740S
2SB941
NJM4558D
NJM5532D-D
PCM56P-K
TC74HC00P
TC74HC08P
LB1294
TD62003AP
UPD4053BC
LB1433N
M5218P-K
M5220P
M5218L
M51951ASL
OUTPUT
GND
INPUT
TC74HC174F
CXA1244S
CXK5816SP-12L
CXK5816SP-15L
CXA1081M
CXD1125QZ
TC17G005AF-0048
UPD7216ACW-051
SM5804D
M5F78M05L
M5F78M06L
I G O
M5F79M05L
M5F79M06L
G I O

DP-990SG

KENWOOD

EXPLODED VIEW (MECHANISM)

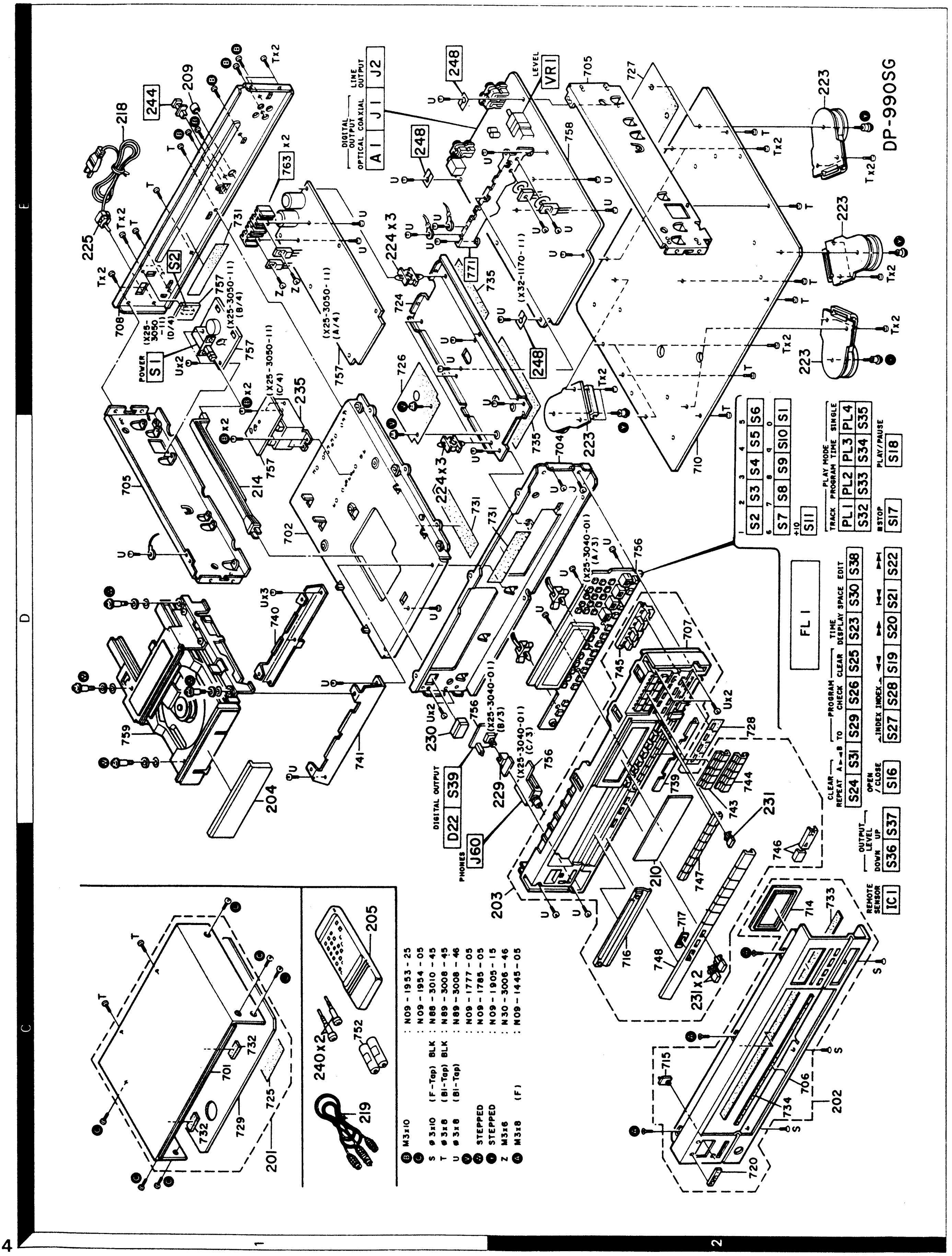
B	M3x10	(BI)	: N35-3010-46
C	⌀2.6x5	(Bi-Tap) BLK	: N89-2605-45
D	⌀2.6x10	(Bi-Tap)	: N89-2610-46
E	M2.6x3		: N09-1849-05
F	⌀2.6x16	(BI-Tap)	: N86-2616-46
G	M2.6x6		: N30-2606-46
H	M2x10	(BI)	: N35-2010-46
J	⌀3x6	(Bi-Tap)	: N86-3006-46
K	M2.6x5	(STEPPED)	: N09-1380-05
L	⌀2.6x6	(BI-Tap)	: N89-2606-46
M	⌀2x6	(Tap)	: N84-2006-46
N	M2x3		: N30-2003-46


A
B
1
2
3
77
18
42
79
14
46
30
47
41
802
29
73
76
17
66
61
87
63
51
88
37x2
12
77
31
54
45
65
64
44
35x2
21
826
803
60
807
57
40
59x2
74x2
56x2
804
13
43
33
55
Lx2
M2
22
75
48
M1
49
58
S3
START LIMIT
818
(J25)(B/3)
36
S2
CLOSE
16
52
62
34
39
26
11
808
813
809
Gx2
32
M3
53
20
19
27
28
S1
OPEN
801
822
(X29-1870-00)
(J25)(C/3)
(J25-5700-03)(A/3)

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)

B	M3x10		: N09-1953-25
C			: N09-1954-05
S	⌀3x10	(F-Tap) BLK	: N88-3010-45
T	⌀3x8	(BI-Tap) BLK	: N89-3008-45
U	⌀3x8	(BI-Tap)	: N89-3008-46
V			: N09-1777-05
W	STEPPED		: N09-1785-05
Y	STEPPED		: N09-1905-15
Z	M3x6		: N30-3006-46
A	M3x8	(F)	: N09-1445-05


DP-990SG
218
244
209
225
S2
763 x2
DIGITAL OUTPUT OPTICAL COAXIAL
LINE OUTPUT
A1
J1
J2
248
LEVEL
VR1
705
727
223
224x3
771
735
758
757
(X25-3050-11)(D/4)
(X25-3050-11)(B/4)
(X25-3050-11)(A/4)
(X25-3050-11)(C/4)
(X32-1170-11)
POWER
S1
235
214
702
726
704
710
724
731
756
(X25-3040-01)(A/3)
(X25-3040-01)(B/3)
(X25-3040-01)(C/3)
740
741
759
204
230
229
DIGITAL OUTPUT
D22
S39
PHONES
J60
203
707
745
728
739
744
743
231
746
747
210
716
748
717
231x2
714
733
715
706
734
720
202
201
729
725
732
701
205
752
240x2
219
FL1
IC1
REMOTE SENSOR
S36
S37
OUTPUT LEVEL DOWN UP
S24
S31
CLEAR REPEAT A→B
S16
OPEN/CLOSE
S29
S26
S25
S23
S30
S38
PROGRAM CHECK CLEAR DISPLAY SPACE EDIT
TIME
S27
S28
S19
S20
S21
S22
INDEX
S2
S3
S4
S5
S6
S7
S8
S9
S10
S1
S11
PL1
PL2
PL3
PL4
S32
S33
S34
S35
TRACK PROGRAM TIME SINGLE
PLAY MODE
S17
STOP
S18
PLAY/PAUSE
Tx2
Ux2
Ux3

Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
				DP-990SG		
201	1C	⁎	A01-1618-12	METALLIC CABINET ASSY		
202	2C	⁎	A20-5345-02	PANEL ASSY		
203	2C	⁎	A22-0914-02	SUB PANEL ASSY		
204	1D	⁎	A29-0123-03	PANEL (TRAY)		
205	1C		A70-0180-05	REMOTE CONTROLLER ASSY		
209	1E		B09-0068-05	CAP (COAXIAL)		
210	2C		B10-0897-04	FRONT GLASS (DISPLAY)		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0094-03	WARRANTY CARD	UUE	
-			B46-0095-03	WARRANTY CARD	UUE	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0121-03	WARRANTY CARD	P	
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-		⁎	B50-8529-00	INSTRUCTION MANUAL(ENGLISH)		
-		⁎	B50-8530-00	INSTRUCTION MANUAL(FRENCH)	PMXE	
-		⁎	B50-8531-00	INSTRUCTION MANUAL(SPANISH)	M	
-		⁎	B50-8532-00	INSTRUCTION MANUAL(G.D.I)	E	
-			B58-0223-04	CAUTION CARD (PRE-SET 120V)	U	
-			B58-0269-04	CAUTION CARD	K	
-			B58-0400-04	CAUTION CARD		
-			B58-0513-04	CAUTION CARD (PRESET220-240)	UE	
-			B58-0849-04	CAUTION CARD		
-			B59-0092-00	SERVICE DIRECTORY	UUE	
214	1D		D21-1395-03	EXTENSION SHAFT(POWER)		
⚠ 218	1E		E30-0459-05	AC POWER CORD	E	
⚠ 218	1E		E30-0780-05	AC POWER CORD	KP	
⚠ 218	1E		E30-0812-05	AC POWER CORD	UMUE	
⚠ 218	1E		E30-1341-05	AC POWER CORD	X	
⚠ 218	1E		E30-1416-05	AC POWER CORD	T	
219	1C		E30-0505-05	AUDIO CORD		
-		⁎	H01-7661-04	ITEM CARTON CASE		
-			H10-3481-02	POLYSTYRENE FOAMED FIXTURE(L)		
-			H10-3482-02	POLYSTYRENE FOAMED FIXTURE(R)		
-			H10-3590-04	POLYSTYRENE FOAMED FIXTURE		
-			H20-0417-14	PROTECTION COVER(460X370X360)	M	
-			H21-0244-04	PROTECTION SHEET		
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
-			H25-0319-04	PROTECTION BAG	KPUUEX	
-			H25-0319-04	PROTECTION BAG	TE	
223	2D,2E		J02-0357-05	INSULATOR ASSY		
224	1D,1E		J19-2855-05	UNIT HOLDER		
⚠ 225	1E		J42-0083-05	POWER CORD BUSHING		
-			J61-0050-15	WIRE BAND		
-			J61-0070-05	WIRE BAND		
229	2D		K27-1514-04	KNOB (BUTTON)DIGITAL OUTPUT		
230	1D		K29-2725-04	KNOB (BUTTON)POWER		
231	2C,2D		K29-2648-04	KNOB (BUTTON)OUTPUT LEVEL,+10		
235	1E		L01-4744-05	POWER TRANSFORMER		
240	1C		N09-1906-05	STEPPED SCREW		

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A	2C		N09-1445-05	SET SCREW (M3X8)		
B	1D,1E		N09-1953-25	MACHINE SCREW (M3X10)TRANS		
C	1C		N09-1954-05	MACHINE SCREW (CASE)		
V	1D,1E		N09-1777-05	SEMS (TAPTITE SCREW) SHEET		
W	1D		N09-1785-05	STEPPED SCREW (MECHA)		
Y	2D,2E	*	N09-1905-15	STEPPED SCREW (FOOT)		
DISPLAY UNIT (X25-3040-01)						
D22	1D		B30-1012-05	LED(SLP-981C-50)DIGITAL OUTPUT		
PL1 -4	2D	*	B30-1207-05	LAMP (PLAY MODE)		
C1 ,2			C91-0085-05	CERAMIC 0.022UF N		
C3			C91-0753-05	CHIP C 470PF K		
C4 ,5			C91-0765-05	CERAMIC 0.0047UF M		
J60	1C		E11-0162-05	PHONE JACK(3P) PHONES		
CP1		*	R90-0498-05	MULTI-COMP 2.2KX4 J 1/8W		
S1 -11	2D		S40-1064-05	PUSH SWITCH (1-0,+10)		
S16 -38	2D		S40-1064-05	PUSH SWITCH (PROGRAM,FF,REW)		
S39	1D		S40-2323-05	PUSH SWITCH (DIGITAL OUTPUT)		
D1 -18			1SS131	DIODE		
D1 -18			1SS178	DIODE		
FL1	2D		CP5322AGNR	FLUORESCENT INDICATOR TUBE		
IC1	2C		BX-1408	IC(REMOTE SENSOR)		
IC2			TC74HC174F	IC(D-FLIP FLOP)		
IC3		*	TD62003AP	IC(DARLINGTON DRIVER)		
D/A CONVERTER UNIT (X25-3050-XX)-01: X, T, E, -11: K, P, -21, U, M, UE						
C1 ,2			C91-0980-05	CERAMIC 15PF G		
C3 ,4			C90-1334-05	NP-ELEC 47UF 10WV		
C5 ,6			C91-0175-05	POLYSTY 56PF K		
C7 ,8			CF92FV1H203J	MF 0.020UF J		
C9 ,10			CF92FV1H332J	MF 3300PF J		
C11 -18			CK45FF1H103Z	CERAMIC 0.010UF Z		
C19 ,20			CF92FV1H182J	MF 1800PF J		
C21 ,22			CE04KW1A101M	ELECTRO 100UF 10WV		
C25 ,26			CF92FV1H242J	MF 2400PF J		
C29 -32			CF92FV1H242J	MF 2400PF J		
C35 ,36			CF92FV1H242J	MF 2400PF J		
C37 ,38			CQ09FS1H151J	POLYSTY 150PF J		
C39 -42			CE04KW1C330M	ELECTRO 33UF 16WV		
C43 ,44			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C47 -50			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C51 ,52			CF92FV1H162J	MF 1600PF J		
C53 ,54			CQ09FS1H471J	POLYSTY 470PF J		
⚠ C55 -57			C91-0647-05	CERAMIC 0.01UF P		
C61 -68			C91-0170-05	POLYSTY 22PF K		
C96 -99			CE04KW1C330M	ELECTRO 33UF 16WV		
C100,101			CE04KW1C332M	ELECTRO 3300UF 16WV		
C102-105			CE04KW1C330M	ELECTRO 33UF 16WV		
C107			CE04KW1A470M	ELECTRO 47UF 10WV		
C108			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C110			CE04KW1A470M	ELECTRO 47UF 10WV		
C111			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C112			CE04KW0J222M	ELECTRO 2200UF 6.3WV		

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C113,114			C91-0769-05	CERAMIC 0.01UF M		
C115			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C120,121			CE04KW1C330M	ELECTRO 33UF 16WV		
C122,123			CE04KW1E221M	ELECTRO 220UF 25WV		
C124,125			CE04KW1E222M	ELECTRO 2200UF 25WV		
C126			CE04KW1A101M	ELECTRO 100UF 10WV		
C127,128			CE04KW1E330M	ELECTRO 33UF 25WV		
C129,130			CE04KW1E222M	ELECTRO 2200UF 25WV		
L1 -6			L40-1021-11	SMALL FIXED INDUCTOR(1.0MH,K)		
L7 -9			L33-0328-05	CHOKE COIL		
⚠ L13			L79-0733-05	LINE FILTER		
L14 -22			L40-1092-17	SMALL FIXED INDUCTOR(1UH,M)		
X1		*	L77-1135-05	CRYSTAL RESONATOR		
R5 ,6			RN14BK2C1001F	RN 1.00K F 1/6W		
R9 ,10			RN14BK2C10R0F	RN 10.0 F 1/6W		
R11 ,12			RN14BK2C1003F	RN 100K F 1/6W		
R13 ,14			RN14BK2C1211F	RN 1.21K F 1/6W		
R15 ,16			RN14BK2C8250F	RN 825.0 F 1/6W		
R19 ,20			RN14BK2C1001F	RN 1.00K F 1/6W		
R23 ,24			RS14KB3D271J	FL-PROOF RS 270 J 2W		
R27 ,28			RN14BK2C1621F	RN 1.62K F 1/6W		
R37 ,38			RN14BK2C9092F	RN 90.9K F 1/6W		
R39 ,40			RN14BK2C1961F	RN 1.96K F 1/6W		
R47 ,48			RN14BK2C6341F	RN 6.34K F 1/6W		
R49 -54			RN14BK2C3241F	RN 3.24K F 1/6W		
R55 ,56			RN14BK2C9092F	RN 90.9K F 1/6W		
R57 ,58			RN14BK2C1961F	RN 1.96K F 1/6W		
R59 -64			RN14BK2C3241F	RN 3.24K F 1/6W		
R65 ,66			RN14BK2C1621F	RN 1.62K F 1/6W		
R69 ,70			RN14BK2C1963F	RN 196K F 1/6W		
R71 ,72			RN14BK2C9092F	RN 90.9K F 1/6W		
R75 -78			RN14BK2C6811F	RN 6.81K F 1/6W		
R79 -82			RN14BK2C1002F	RN 10.0K F 1/6W		
R83 ,84			RN14BK2C1003F	RN 100K F 1/6W		
R85 ,86			RN14BK2C1002F	RN 10.0K F 1/6W		
R89 ,90			RN14BK2C1001F	RN 1.00K F 1/6W		
R95		*	RN14BK2C1004F	RN 1.00M F 1/6W		
VR1 ,2		*	R12-1100-05	TRIMMING POT.(2.2K)DAC OUTPUT		
VR3 ,4		*	R12-3147-05	TRIMMING POT.(47K) DAC WARP		
VR5 ,6		*	R12-1102-05	TRIMMING POT. (DAC WARP)		
K1 ,2			S51-2074-05	MAGNETIC RELAY		
S1	1E		S40-1103-05	PUSH SWITCH (POWER TYPE)		
S2	1E		S31-2128-05	SLIDE SWITCH (POWER TYPE)	UMUE	
PH1			T95-0101-05	OPTO ISOLATOR		
D1 -8			DSM1A1	DIODE		
D9			HZS5.1S(B2)	ZENER DIODE		
D9			RD5.1JS(B2)	ZENER DIODE		
D10 -13			1SS133	DIODE		
D10 -13			1SS176	DIODE		
D14		*	HZS11N(B2)	ZENER DIODE		
D14		*	RD11ES(B2)	ZENER DIODE		
D15 ,16		*	HZS20S(B2)	ZENER DIODE		
D15 ,16		*	RD20JS(B2)	ZENER DIODE		

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D17			E-102	CONSTANT CURRENT DIODE		
D18 -21			1SS133	DIODE		
D18 -21			1SS176	DIODE		
IC1 ,2			PCM56P-K	IC(DA CONVERTER)		
IC3 ,4			NJM5532D-D	IC(OP AMP X2)		
IC5 -10			NJM4560D-A	IC(OP AMP X2)		
IC13			M5220P	IC(OP AMP X2)		
IC14			SM5804D	IC(DIGITAL FILTER)		
IC15			TC17G005AF-0048	IC(VCXO)		
IC16		*	M5F79M06L	IC(VOLTAGE REGULATOR/ -6V)		
IC17		*	M5F78M06L	IC(VOLTAGE REGULATOR/ +6V)		
IC22			M5F79M05L	IC(VOLTAGE REGULATOR/ -5V)		
IC23			M5F78M05L	IC(VOLTAGE REGULATOR/ +5V)		
IC24			M51951ASL	IC(SYSTEM RESET)		
Q2			2SD1266(P)	TRANSISTOR		
Q3			2SB941(P)	TRANSISTOR		
Q10 ,11			DTC114YFF	DIGITAL TRANSISTOR		
Q12 ,13			DTC143EFF	DIGITAL TRANSISTOR		
Q14			2SA733(A)(Q,P)	TRANSISTOR		
Q14			2SA999(E,F)	TRANSISTOR		
CONTROL CIRCUIT UNIT (X29-1870-00)						
C1			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C2			CE04KW1A470M	ELECTRO 47UF 10WV		
C3			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C4			CE04KW1A470M	ELECTRO 47UF 10WV		
C5			CF92FV1H333J	MF 0.033UF J		
C6			CF92FV1H102J	MF 1000PF J		
C7			CF92FV1H104J	MF 0.10UF J		
C8			CK45FF1H103Z	CERAMIC 0.010UF Z		
C9 ,10			C91-0725-05	CERAMIC 15PF J		
C11			CF92FV1H222J	MF 2200PF J		
C13			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C14			C91-0700-05	CERAMIC 0.1UF J		
VR1 ,2		*	R12-3071-05	TRIMMING POT.(10K)FO/TR GAIN		
VR3 ,4			R12-3072-05	TRIMMING POT. (FO/TR ERROR)		
IC1		*	CXA1081M	IC(RF AMP)		
IC2			TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
Q1			2SC2878	TRANSISTOR		
CD PLAYER UNIT (X32-1170-11)						
244	1E		B09-0063-05	CAP		
C1			C91-0729-05	CERAMIC 22PF J		
C2			CF92FV1H104J	MF 0.10UF J		
C3			CC45FSL1H180J	CERAMIC 18PF J		
C4			C90-1349-05	NP-ELEC 1UF 50WV		
C5			CF92FV1H394J	MF 0.39UF J		
C6			CF92FV1H103J	MF 0.010UF J		
C7			CC45FSL1H150J	CERAMIC 15PF J		
C8			CK45FF1H223Z	CERAMIC 0.022UF Z		
C9			C91-0085-05	CERAMIC 0.022UF N		
C10			C90-1350-05	NP-ELEC 2.2UF 50WV		
C11			CF92FV1H104J	MF 0.10UF J		
C12			C91-0749-05	CERAMIC 220PF K		
C13			CC45FSL1H151J	CERAMIC 150PF J		

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C14			CC45FSL1H020C	CERAMIC 2.0PF C		
C15			CF92FV1H683J	MF 0.068UF J		
C16			CF92FV1H474J	MF 0.47UF J		
C17			CC45FSL1H151J	CERAMIC 150PF J		
C18			CF92FV1H473J	MF 0.047UF J		
C19			CF92FV1H393J	MF 0.039UF J		
C20			CF92FV1H154J	MF 0.15UF J		
C21			CC45FSL1H080D	CERAMIC 8.0PF D		
C22			CF92FV1H154J	MF 0.15UF J		
C23			CK45FF1H223Z	CERAMIC 0.022UF Z		
C24			C91-0085-05	CERAMIC 0.022UF N		
C25			CF92FV1H103J	MF 0.010UF J		
C26			C90-1333-05	NP-ELEC 22UF 10WV		
C27			CF92FV1H272J	MF 2700PF J		
C28			C90-1331-05	NP-ELEC 0.47UF 50WV		
C29			CK45FF1H223Z	CERAMIC 0.022UF Z		
C30			C91-0085-05	CERAMIC 0.022UF N		
C31 -34			CE04KW1A470M	ELECTRO 47UF 10WV		
C35			CK45FF1H223Z	CERAMIC 0.022UF Z		
C36			C91-0085-05	CERAMIC 0.022UF N		
C37 ,38			CE04KW1C330M	ELECTRO 33UF 16WV		
C39 ,40			C90-1349-05	NP-ELEC 1UF 50WV		
C41			C91-0085-05	CERAMIC 0.022UF N		
C42			C90-1349-05	NP-ELEC 1UF 50WV		
C43 ,44			CF92FV1H103J	MF 0.010UF J		
C45 ,46			CE04KW1C330M	ELECTRO 33UF 16WV		
C47			CF92FV1H222J	MF 2200PF J		
C48			CC45FUJ1H330J	CERAMIC 33PF J		
C49			CC45FSL1H221J	CERAMIC 220PF J		
C50			CC45FUJ1H050C	CERAMIC 5.0PF C		
C51 ,52			CF92FV1H472J	MF 4700PF J		
C53			CF92FV1H563J	MF 0.056UF J		
C54			CC45FSL1H101J	CERAMIC 100PF J		
C55			CF92FV1H223J	MF 0.022UF J		
C56			CK45FF1H223Z	CERAMIC 0.022UF Z		
C57			CE04KW1A470M	ELECTRO 47UF 10WV		
C58			CE04KW1C331M	ELECTRO 330UF 16WV		
C59			CE04KW1H221M	ELECTRO 220UF 50WV		
C60			CK45FF1H223Z	CERAMIC 0.022UF Z		
C61			CE04KW1A470M	ELECTRO 47UF 10WV		
C62			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C63			CE04KW1A470M	ELECTRO 47UF 10WV		
C64 ,65			CE04KW1C332M	ELECTRO 3300UF 16WV		
C66			CE04KW1C330M	ELECTRO 33UF 16WV		
C67			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C68 ,69			CE04KW1C330M	ELECTRO 33UF 16WV		
C70			CE04KW0J221M	ELECTRO 220UF 6.3WV		
C71			CE04KW1A470M	ELECTRO 47UF 10WV		
C72			CK45FF1H223Z	CERAMIC 0.022UF Z		
C73			CE04KW1C330M	ELECTRO 33UF 16WV		
C74			CE04KW1A470M	ELECTRO 47UF 10WV		
C75			CE04KW1A101M	ELECTRO 100UF 10WV		
C76			C91-0757-05	CERAMIC 0.001UF K		
C77			CK45FF1H223Z	CERAMIC 0.022UF Z		
C78			C91-0757-05	CERAMIC 0.001UF K		

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C79			CE04KW1A470M	ELECTRO 47UF 10WV		
C80			CK45FF1H223Z	CERAMIC 0.022UF Z		
C81			C91-0085-05	CERAMIC 0.022UF N		
C82 -86			CK45FF1H223Z	CERAMIC 0.022UF Z		
C87			CE04KW1A470M	ELECTRO 47UF 10WV		
C88			C91-0085-05	CERAMIC 0.022UF N		
C89			CK45FB1H102K	CERAMIC 1000PF K		
C90			CK45FF1H223Z	CERAMIC 0.022UF Z		
C91			CE04KW1H101M	ELECTRO 100UF 50WV		
C92			CK45FF1H223Z	CERAMIC 0.022UF Z		
C93			CE04KW1H3R3M	ELECTRO 3.3UF 50WV		
C94			CE04KW1A470M	ELECTRO 47UF 10WV		
C95			C91-0085-05	CERAMIC 0.022UF N		
C96			C91-0757-05	CERAMIC 0.001UF K		
C97			CK45FF1H223Z	CERAMIC 0.022UF Z		
C98			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C99			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C100,101			CF92FV1H332J	MF 3300PF J		
C102,103			CC45FSL1H221J	CERAMIC 220PF J		
C104,105			CE04KW1C220M	ELECTRO 22UF 16WV		
C106,107			CE04KW1A101M	ELECTRO 100UF 10WV		
C108,109			CC45FSL1H680J	CERAMIC 68PF J		
C110,111			CE04KW1A101M	ELECTRO 100UF 10WV		
C112,113			C91-0085-05	CERAMIC 0.022UF N		
C114			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C115			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C116,117			CE04KW1E330M	ELECTRO 33UF 25WV		
248	1E,2E		E23-0149-05	TERMINAL		
J1	1E		E13-0131-05	PHONO JACK (DIGITAL OUT)		
J2	1E		E13-0483-05	PHONO JACK (LINE OUTPUT)		
L1 ,2			L40-1021-14	SMALL FIXED INDUCTOR(1.0MH,K)		
L3 -8			L33-0328-05	CHOKE COIL		
L9			L32-0328-15	OSCILATING COIL		
L10			L39-0155-05	MATCHING COIL		
L11 -13			L40-1092-17	SMALL FIXED INDUCTOR(1UH,M)		
L14			L40-1092-17	SMALL FIXED INDUCTOR(1UH,M)		
CP1			R90-0202-05	MULTI-COMP 47KX4 J 1/6W		
CP2 ,3			R90-0272-05	MULTI-COMP 100KX12 J 1/6W		
CP4			R90-0278-05	MULTI-COMP 100KX7 J 1/6W		
CP5			R90-0453-05	MULTI-COMP 4.7K J 1/6W		
R21 ,22			RS14DB3D100J	FL-PROOF RS 10 J 2W		
R40 ,41			RS14DB3D100J	FL-PROOF RS 10 J 2W		
R49 ,50			RS14DB3D5R6J	FL-PROOF RS 5.6 J 2W		
R56			RS14DB3D100J	FL-PROOF RS 10 J 2W		
R62			RS14DB3D100J	FL-PROOF RS 10 J 2W		
R73 ,74			RS14DB3D6R8J	FL-PROOF RS 6.8 J 2W		
R140-143			RN14BK2C1000F	RN 100.0 F 1/6W		
R144,145			RN14BK2C1003F	RN 100K F 1/6W		
R146,147			RN14BK2C1001F	RN 1.00K F 1/6W		
R148,149			RN14BK2C1002F	RN 10.0K F 1/6W		
R150,151			RN14BK2C3831F	RN 3.83K F 1/6W		
R152,153			RN14BK2C10R0F	RN 10.0 F 1/6W		
R154-157		*	RN14BK2E10R0F	RN 10.0 F 1/4W		

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R158,159		*	RN14BK2E56R2F	RN 56.2 F 1/4W		
VR1	2E		R29-1001-05	POTENTIOMETER (LEVEL)		
D1			1SS133	DIODE		
D1			1SS176	DIODE		
D2			1SV147	VARISTOR		
D3 -6			1SS133	DIODE		
D3 -6			1SS176	DIODE		
D7			HZS7.5S(B)	ZENER DIODE		
D7			RD7.5JS(B)	ZENER DIODE		
D8			HZS8.2N(B2)	ZENER DIODE		
D8			RD8.2ES(B2)	ZENER DIODE		
D9			1SS131	DIODE		
D9			1SS178	DIODE		
D10 -12			DSM1A1	DIODE		
D13			RD33JS(B)	ZENER DIODE		
D14 -17			DSM1A1	DIODE		
D18 -28			1SS176	DIODE		
D29 ,30			E-272	CONSTANT CURRENT DIODE		
D31 ,32			MA27W	VARISTOR		
D33			1SS133	DIODE		
D33			1SS176	DIODE		
IC1			CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC2			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
IC3			M5218P-K	IC(OP AMP X2)		
IC4			NJM4558D	IC(OP AMP X2)		
IC5			M5218P-K	IC(OP AMP X2)		
IC6			CXD1125QZ	IC(DIGITAL SIGNAL PROCESSOR)		
IC7			CXK5816SP-12L	IC(2KX8 RAM)		
IC7			CXK5816SP-15L	IC(2KX8 RAM)		
IC9			TC74HC08P	IC(AND X2)		
IC10			UPD75216ACW-051	IC(MICROPROCESSOR)		
IC11			M51951ASL	IC(SYSTEM RESET)		
IC12			LB1433N	IC(LEVEL METER DRIVER)		
IC13-17			LB1294	IC(6CH DARLINGTON DRIVER)		
IC18			M5F78M05L	IC(VOLTAGE REGULATOR/ +5V)		
IC19			M5218L	IC(OP AMP X2)		
IC20			NJM4558D	IC(OP AMP X2)		
Q1			2SC2878	TRANSISTOR		
Q2			2SC3940A	TRANSISTOR		
Q3			2SA1534A	TRANSISTOR		
Q4			2SC3940A	TRANSISTOR		
Q5			2SA1534A	TRANSISTOR		
Q6			2SC3940A	TRANSISTOR		
Q7			2SA1534A	TRANSISTOR		
Q8			2SC3940A	TRANSISTOR		
Q9			2SA1534A	TRANSISTOR		
Q10			2SD1266	TRANSISTOR		
Q11			2SB941	TRANSISTOR		
Q12			2SD1266	TRANSISTOR		
Q13			2SA1110	TRANSISTOR		
Q14			2SC2003	TRANSISTOR		
Q15			2SC1740S(Q,R)	TRANSISTOR		
Q15			2SC945(A)(Q,P)	TRANSISTOR		
Q16			2SA733(A)(Q,P)	TRANSISTOR		

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Q16			2SA933S(Q,R)	TRANSISTOR		
Q17			2SD1266	TRANSISTOR		
Q18 ,19			2SA954	TRANSISTOR		
Q20			2SC3940A	TRANSISTOR		
Q21 ,22			2SD882	TRANSISTOR		
Q23 ,24			2SB772	TRANSISTOR		
Q25 ,26			DTA124EN	DIGITAL TRANSISTOR		
A1	1E		W02-0784-05	ELECTRIC CIRCUIT MODULE		
MECHANISM ASS'Y (X92-1210-01)						
C1			C90-1349-05	NP-ELEC 1UF 50WV		
C2 ,3			C91-0085-05	CERAMIC 0.022UF N		
1	2A	⋇	D02-0073-04	TURNTABLE PLATTER		
11	3B	⋇	D13-0657-05	GEAR ASSY		
12	2A		D10-1266-03	SLIDER (L)		
13	2B		D10-1267-03	SLIDER (R)		
14	1A		D10-1268-03	SLIDER		
16	3B	⋇	D10-2011-04	ROD		
17	1B		D10-1271-03	ARM		
18	1A		D12-0105-15	CAM		
19	3A		D13-0159-08	GEAR		
20	3A		D13-0160-08	GEAR		
21	2A		D13-0161-03	GEAR		
22	3A	⋇	D13-0640-08	GEAR		
26	3A		D14-0162-04	ROLLER		
27	3A		D15-0220-08	PULLEY		
28	3A	⋇	D16-0169-08	BELT		
29	1B		D21-1051-04	SHAFT		
30	1B		D21-1052-04	SHAFT		
31	2A		D32-0122-04	STOPPER		
32	3A	⋇	D40-0583-05	DRIVE MECHANISM ASSY(LOADING)		
33	2A	⋇	D40-0582-05	DRIVE MECHANISM ASSY(FEED)		
34	3A		F07-0503-04	COVER		
35	2A	⋇	G16-0160-04	SHEET		
36	3B	⋇	G01-2104-04	COMPRESSION SPRING		
37	2A,2B	⋇	G11-1238-04	CUSHION		
39	3A		G13-0189-04	CUSHION (CHASSIS)		
40	2A	⋇	G01-2105-04	COMPRESSION SPRING(TURNTABLE)		
41	1B		G01-0675-04	COMPRESSION SPRING		
42	1A,1B	⋇	G01-2102-04	EXTENSION SPRING		
43	2B		G01-1524-04	EXTENSION SPRING(FRONT-L)		
44	2A		G01-1525-04	EXTENSION SPRING		
45	2A,2B		G13-0166-04	CUSHTON (TRAY)		
46	1B		G16-0117-04	SHEET (38X38X2)		
47	1B		G16-0134-04	SHEET (38X152X1)		
48	2A,3A	⋇	G01-2181-04	COMPRESSION SPRING		
49	3B	⋇	G16-0162-04	SHEET (LR DAMPER)		
51	1A	⋇	J11-0104-03	CLAMPER		
52	2B,3B	⋇	J21-5092-04	MOUNTING HARDWARE		
53	3A	⋇	J21-5098-08	MOUNTING HARDWARE ASSY		
54	2A		J21-3509-03	MOUNTING HARDWARE ASSY		
55	2A	⋇	J21-5097-08	MOUNTING HARDWARE ASSY		
56	2A,2B		J02-0192-05	INSULATOR		

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57	2A	⋇	J19-2874-04	HOLDER (TURNTABLE)		
58	3A,3B		J42-0142-04	BUSHING (CHASSIS)		
59	2A,2B		J31-0282-04	COLLAR		
60	2A		J90-0143-03	GUIDE (STOPPER)		
61	1A		J90-0157-03	RAIL		
62	2B	⋇	J91-0341-05	PICKUP		
63	1B		J99-0024-12	TRAY		
64	2B		J99-0025-13	TRAY		
65	2B		J99-0026-13	TRAY		
66	3A,1B	⋇	J19-2875-14	HOLDER		
-			J61-0307-05	WIRE BAND		
73	1A		N15-1026-45	FLAT WASHER (Ø2.6)		
74	2A,2B		N19-1072-04	FLAT WASHER		
75	3A		N19-0366-04	FLAT WASHER (Ø2.1)		
76	1A		N19-0945-04	FLAT WASHER (YOKE)		
77	1A,3A		N19-0891-04	FLAT WASHER (CHASSIS)		
79	1A,1B		N29-0207-04	RETAINING RING (Ø2.5)		
E	2A	⋇	N09-1849-05	SET SCREW (M2.6X3)		
K	2A,2B		N09-1380-05	STEPPED SCREW (M2.6X5)		
S1 ,2	3A,3B		S46-1045-05	LEAF SWITCH (OPEN/CLOSE)		
S3	3A		S40-1101-05	PUSH SWITCH (START LIMIT)		
87	1A		T50-1036-04	YOKE		
88	1B		T99-0222-05	MAGNET		
M1	2A	⋇	T42-0439-05	DC MOTOR (DISC)		
M2	2A	⋇	T42-0437-08	MOTOR ASSY (FEED)		
M3	3A	⋇	T42-0438-08	MOTOR ASSY (LOADING)		

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SPECIFICATIONS

[Format]

Type:	Compact disc player
Read system:	Non-contact optical pickup
Laser:	GaAlAs, wave-length = 780nm, 3-beam tracking
Rotational speed:	About 500 to 200 rpm
Error correction:	Cross Interleave Read-Solomon code
Audio channels:	2

[Audio]

Frequency response:	4Hz ~ 20kHz
Signal-to-noise ratio:	more than 106dB
Total harmonic distortion:	0.0015% at 1kHz
Channel separation:	more than 104dB at 1kHz
Wow flutter:	Below measurable limit
Output voltage	
Analog outputs	
LINE OUT (FIXED):	2.0V
LINE OUT (VARIABLE):	0 ~ 2.0V
Digital output	
Coax cable terminal:	0.5V p-p, 75 ohms
Optical output:	−15dBm ~ −25dBm
Headphone jack:	60mW (8 ohms)

[General]

Power consumption:	23W
Dimensions:	W: 440mm (17-5/16″) H: 124mm (4-7/8″) D: 360mm (14-3/16″)
Weight:	10.8kg (23.8 lb)

[Wireless remote control unit]

Model:	RC-P1100SG
Type:	Infrared pulse
Power supply:	DC 3V (two AA size batteries)
Weight:	115g (0.253 lb) (with batteries)

[Supplied accessories]

Connection cord:	1 stereo cord
Wireless remote control (RC-P1100SG):	1
Batteries (AA):	2

Note:
We follow a policy of continuous development.
For this reason specifications may be changed without notice.

Note:
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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